TEXAS INSTRUMENTS

# High-Performance FIFO Memories

## Application and Data Manual


1993

# *High-Performance FIFO Memories Application and Data Manual*

*1993 Rev. II*

TEXAS INSTRUMENTS

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## INTRODUCTION

First-In, First-Out (FIFO) memories from Texas Instruments are valuable data path elements for eliminating bottlenecks and regulating flow. Data transfers in and out of a FIFO memory are independent of one another and allow the device to be the communication medium between two asynchronous systems. Empty and full status flags that prevent underflow and overflow conditions are standard with all devices, and many have programmable almost full/almost empty flags to optimize the control of a particular system.

Each FIFO is constructed with a dual-port SRAM, read and write address incrementing logic, and flag circuitry. Rising-edge-triggered clocks are featured on all TI FIFOs, with self-timed reads and writes on memory that allow a large variance of usable pulse widths. The *strobed* style of FIFO produced by TI writes data to memory on each low-to-high transition of the load clock (LDCK) input and reads data on each rising edge of the unload clock (UNCK) input.

TI's *clocked* style FIFO can also receive asynchronous clocks for writing and reading data, but the clock inputs are designed to be continuous, with the rising edge affecting data transfers when separate enable signals are asserted. This characteristic allows a seamless interface between the device and other high-speed buses or microprocessors with similar control. The availability of the free-running clock also provides the means to synchronize the full and empty status flags for use as reliable control signals and reduce the amount of external support logic. Each TI clocked FIFO has its empty flag synchronized to the read clock and its full flag synchronized to the write clock with at least two flip-flop stages. Clocked FIFOs produced in Advanced CMOS technology can support clock frequencies up to 67 MHz, and the SN74ABT7819, the first FIFO produced in Advanced BiCMOS technology, is capable of speeds up to 80 MHz. The SN74ABT7819 is also a bidirectional FIFO, with two independent FIFO memories combined on one chip to buffer data in opposite directions.

Memory organization of the FIFOs ranges in depth from 16 words to 2048 words and data bit widths of 4, 5, 8, 9, and 18. To accommodate the need of reducing the package area as data widths increase, many TI FIFO memories are offered in *shrink* surface-mount packages. The SSOP and SQFP packages, with 25-mil and 0.5-mm lead pitch, respectively, can reduce the FIFO-dedicated board area by 70% over PLCC packages.

Texas Instruments continues to offer leading-edge solutions to customers' needs in both packaging technology and device architecture. This is evidenced by the 120-pin SQFP with 16 mm × 16 mm area used to house the upcoming 32- and 36-bit products. With features such as synchronous retransmit, mailbox bypass registers, byte swapping, and bus-width matching, these devices provide a high level of integration in a compact area for applications such as interfacing a digital signal processor (DSP) to a host processor and matching systems with different memory organizations.

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# Contents

## Introduction

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

## operating conditions and characteristics (in sequence by letter symbols)

**$C_i$** **Input capacitance**
The internal capacitance at an input of the device.

**$C_o$** **Output capacitance**
The internal capacitance at an output of the device.

**$C_{pd}$** **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

**$f_{max}$** **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

**$I_{CC}$** **Supply current**
The current into* the $V_{CC}$ supply terminal of an integrated circuit.

**$\Delta I_{CC}$** **Supply current change (ACT devices only)**
The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

**$I_{IH}$** **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

**$I_{IL}$** **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

**$I_{OH}$** **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

**$I_{OL}$** **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

**$I_{OZ}$** **Off-state (high-impedance-state) output current (of a 3-state output)**
The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

**$t_a$** **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

*Current out of a terminal is given as a negative value.

## operating conditions and characteristics (continued)

**$t_{dis}$** **Disable time (of a 3-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or $t_{PLZ}$. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

**$t_{en}$** **Enable time (of a 3-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{G}$). For 3-state outputs, $t_{en} = t_{PZH}$ or $t_{PZL}$. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them $t_{en} = t_{PHL}$.

**$t_h$** **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

**$t_{pd}$** **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or $t_{PLH}$).

**$t_{PHL}$** **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

**$t_{PHZ}$** **Disable time (of a 3-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state.

**$t_{PLH}$** **Propagation delay time, low-to-high level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

**$t_{PLZ}$** **Disable time (of a 3-state output) from low level**
The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state.

**$t_{PZH}$** **Enable time (of a 3-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level .

**$t_{PZL}$** **Enable time (of a 3-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level .

## operating conditions and characteristics (continued)

$t_{su}$ **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

$t_w$ **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

$V_{IH}$ **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

$V_{IL}$ **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

$V_{OH}$ **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

$V_{OL}$ **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

$V_{T+}$ **Positive-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, $V_{T-}$.

$V_{T-}$ **Negative-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $V_{T+}$.

## definitions

***clocked FIFO***

A first-in, first-out memory that allows data to be written to its array and read from its array at independent rates. The low-to-high transition of a continous (free-running) write clock stores data in memory when write enable input signals are asserted. The low-to-high and high-to-low transitions of the input ready flag (or full flag) output are synchronous to the rising edge of the write clock. The low-to-high transition of a continous (free-running) read clock reads data from memory when read enable input signals are asserted. The low-to-high and high-to-low transitions of the output ready flag (or empty flag) output are synchronous to the rising edge of the read clock.

## function tables

The following symbols are used in function tables on TI data sheets.

| | | |
|---|---|---|
| H | = | high level (steady state) |
| L | = | low level (steady state) |
| ↑ | = | transition from low to high level |
| ↓ | = | transition from high to low level |
| ⟶ | = | value/level or resulting value/level is routed to indicated destination |
| ↶ | = | value/level is re-entered |
| X | = | irrelevant (any input, including transitions) |
| Z | = | off (high-impedance) state of a 3-state output |
| a..h | = | the level of steady-state inputs A through H respectively |
| $Q_0$ | = | level of Q before the indicated steady-state input conditions were established |
| $\overline{Q}_0$ | = | complement of $Q_0$ or level of $\overline{Q}$ before the indicated steady-state input conditions were established |
| $Q_n$ | = | level of Q before the most recent active transition indicated by ↓ or ↑ |
| ⎍ | = | one high-level pulse |
| ⎾ | = | one low-level pulse |
| TOGGLE | = | each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑ |

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, $Q_0$, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎾, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

**function tables (continued)**

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

**FUNCTION TABLE**

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLEAR | MODE | | CLOCK | SERIAL | | PARALLEL | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | S1 | S0 | | LEFT | RIGHT | A | B | C | D | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | H | H | H | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | X | L | L | L | L | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | X | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output $Q_A$, data entered at B will be at $Q_B$, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at $Q_A$ is now at $Q_B$, the previous levels of $Q_B$ and $Q_C$ are now at $Q_C$ and $Q_D$, respectively, and the data previously at $Q_D$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at $Q_B$ is not at $Q_A$, the previous levels of $Q_C$ and $Q_D$ are now at $Q_B$ and $Q_C$, respectively, and the data previously at $Q_A$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

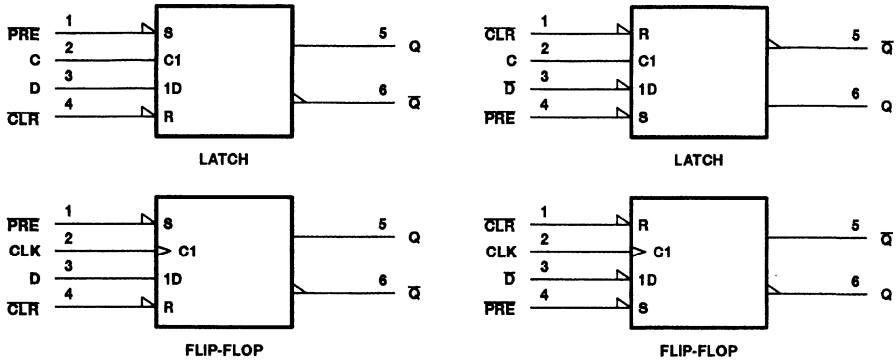
The function table functional tests do not reflect all possible combinations or sequential modes.

## D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producting complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.




The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

## thermal information

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$TJ = R_{\theta JA} \times P_T + T_A \qquad (1)$$

where:

$T_J$ = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
$P_T$ = total power dissipation of the device
$T_A$ = free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.

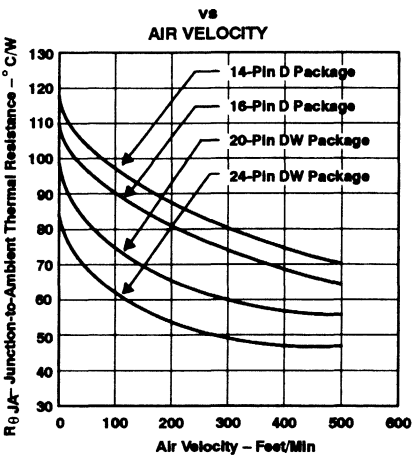



Figure 1

$$P_T = V_{CC} \times I_{CC} + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \qquad (2)$$

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \qquad (3)$$

where:

$V_{CC}$ = supply voltage (5 V for typical, 5.5 V for maximum) (see Note 1)
$I_{CC}$ = quiescent supply current (specified on device data sheet)
$C_{pd}$ = power dissipation capacitance (from the device data sheet)
$f_i$ = input frequency
$C_L$ = output load capacitance
$f_o$ = output frequency
N = number of inputs driven by a TTL device
dc = duty cycle
$\Delta I_{CC}$ = increase in supply current (specified on device data sheet)

NOTE 1: In system applications, $I_{CC}$ can be minimized by keeping input voltage levels less than 1 V for $V_{IL}$ and greater than $V_{CC}$–1 V for $V_{IH}$ and input rise and fall times less than 15 ns.

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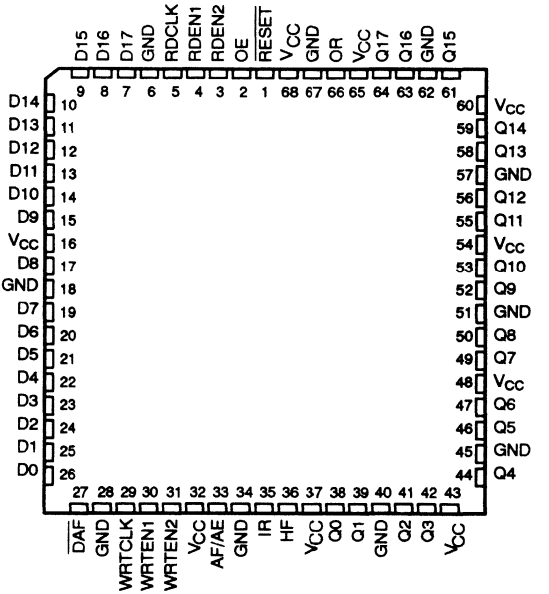
SCAS111–D3489, APRIL 1990–REVISED MAY 1991

- Member of the Texas Instruments *Widebus*™ Family
- Independent Asynchronous Inputs and Outputs
- 1024 Words × 18 Bits
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost Full/Almost Empty Flag
- Input Ready, Output Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 15 ns With a 50-pF Load
- High Output Drive for Direct Bus Interface
- 3-State Outputs
- Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat Pack (PN)

FN PACKAGE
(TOP VIEW)

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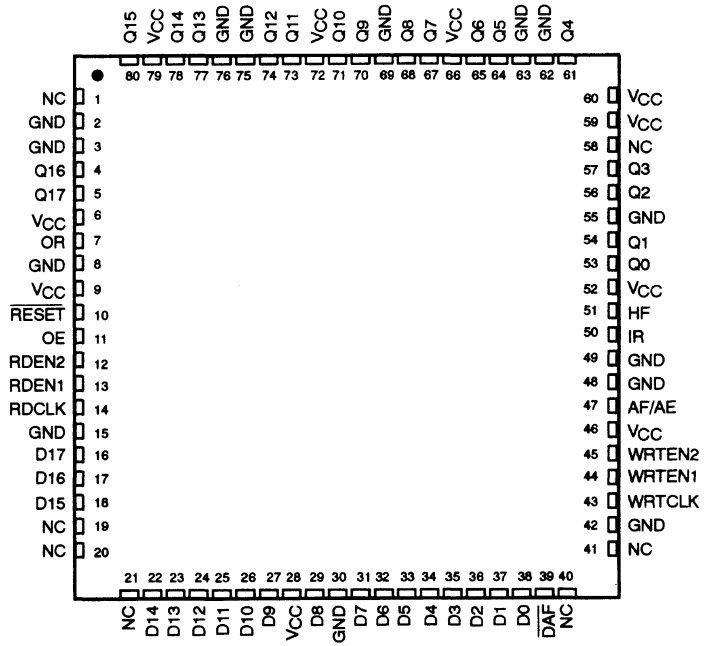
PN PACKAGE
(TOP VIEW)



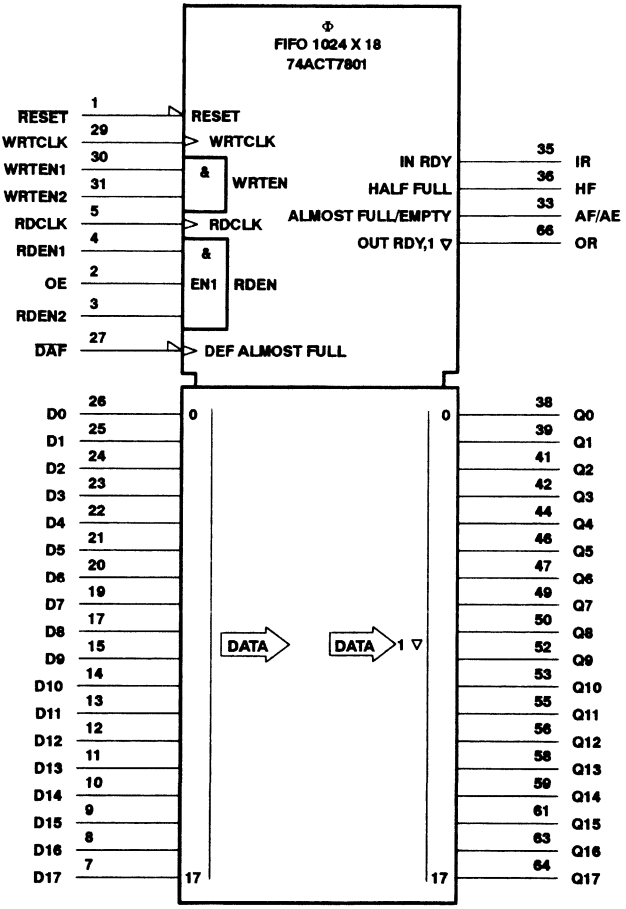

NC – No internal connection

## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7801 is a 1024- × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

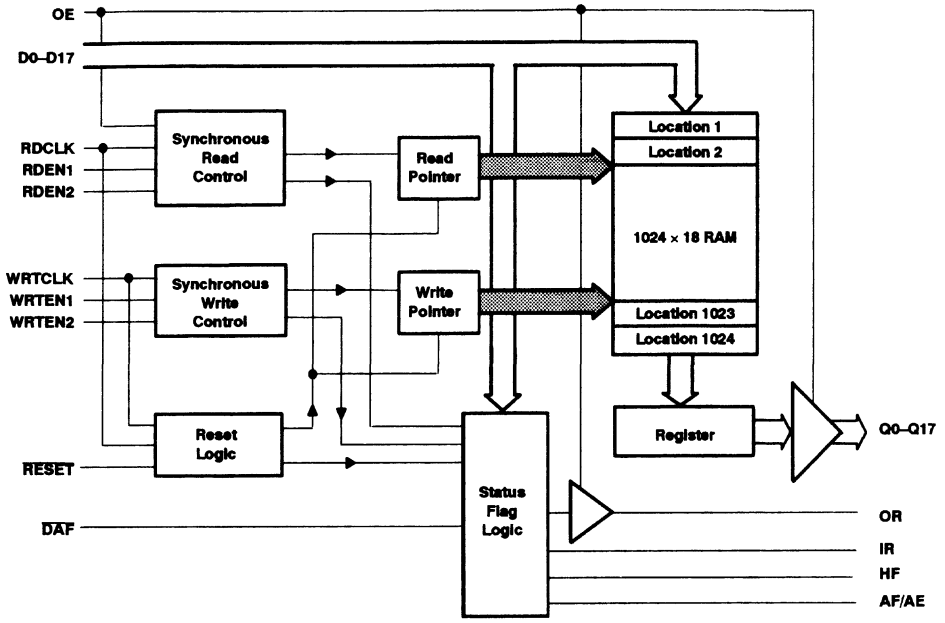
The SN74ACT7801 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts, requests) to their respective system clock.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

## functional block diagram




## functional description

### inputs

#### data in (D0–D17)

Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0-D8 also carry the almost full/almost empty offset value (X) on a high-to-low transition of the define almost full ($\overline{DAF}$) input.

#### reset ($\overline{RESET}$)

A reset is accomplished by taking reset ($\overline{RESET}$) low and generating a minimum of four read clock (RDCLK) and write clock (WRTCLK) cycles. This ensures that the internal read and write pointers are reset and that the output ready flag (OR), the half-full flag (HF), and the input ready flag (IR) are low; the almost full/almost empty flag (AF/AE) is high. The FIFO must be reset upon power up. With the define almost full ($\overline{DAF}$) input at a low level, a low pulse on $\overline{RESET}$ defines the AF/AE status flag using the almost full/almost empty offset value (X), where X is the value previously stored. With $\overline{DAF}$ at a high level, a low-level pulse on $\overline{RESET}$ defines the AF/AE flag using the default value of X = 256.

#### write enables (WRTEN1, WRTEN2)

The write enables (WRTEN1, WRTEN2) must be high before the rising edge of write clock (WRTCLK) for a word to be written into memory. The write enables do not affect the storage of the almost full/almost empty offset value (X).

## functional description (continued)

**write clock (WRTCLK)**

Data is written into memory on a low-to-high transition of the write clock (WRTCLK) if the input ready flag output (IR) and the write enable control inputs (WRTEN1, WRTEN2) are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. The IR flag output is also driven synchronously with respect to the WRTCLK signal.

**read enables (RDEN1, RDEN2)**

Both read enables (RDEN1, RDEN2) must be high before the rising edge of read clock (RDCLK) to read a word out of memory. The read enables are not used to read the first word stored in memory.

**read clock (RDCLK)**

Data is read out of memory on a low-to-high transition at the read clock (RDCLK) input if the output ready flag output (OR) and the output enable (OE) and read enable (RDEN1, RDEN2) control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. The OR flag is also driven synchronously with respect to the RDCLK signal.

**define almost full ($\overline{DAF}$)**

The high-to-low transition of the define almost full ($\overline{DAF}$) input stores the binary value of data inputs D0–D8 as the almost full/almost empty offset value (X). With $\overline{DAF}$ held low, a low pulse on the reset ($\overline{RESET}$) input defines the almost full/almost empty flag (AF/AE) using X.

**output enable (OE)**

The data out (Q0–Q17) outputs and the output ready flag (OR) are in the high-impedance state when the output enable (OE) input is low. OE must be high before the rising edge of read clock (RDCLK) to read a word from memory.

**outputs**

**data out (Q0–Q17)**

The first data word to be loaded into the FIFO is moved to the data out (Q0–Q17) register on the rising edge of the third read clock (RDCLK) pulse to occur after the first valid write. The read enable (RDEN1, RDEN2) inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, and the output ready flag (OR) are high.

**input ready flag (IR)**

The input ready flag (IR) is high when the FIFO is not full and low when the device is full. During reset, the IR flag is driven low on the rising edge of the second write clock (WRTCLK) pulse. The IR flag is driven high on the rising edge of the second WRTCLK pulse after $\overline{RESET}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.

**output ready flag (OR)**

The output ready flag (OR) is high when the FIFO is not empty and low when it is empty. During reset, the OR flag is set low on the rising edge of the third read clock (RDCLK) pulse. The OR flag is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.

**half-full status flag (HF)**

The half-full flag (HF) is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.

## functional description (continued)

### almost full/almost empty status flag (AF/AE)

The almost full/almost empty flag (AF/AE) is defined by the almost full/almost empty offset value (X). The AF/AE flag is high when the FIFO contains (X + 1) or less words or (1025 – X) or more words. The AF/AE flag is low when the FIFO contains between (X + 2) and (1024 – X) words.

### programming procedure for AF/AE

The almost full/almost empty flag (AF/AE) is programmed during each reset cycle. The almost full/almost empty offset value (X) is either a user-defined value or the default value of X = 256. Below are instructions to program AF/AE using both methods.

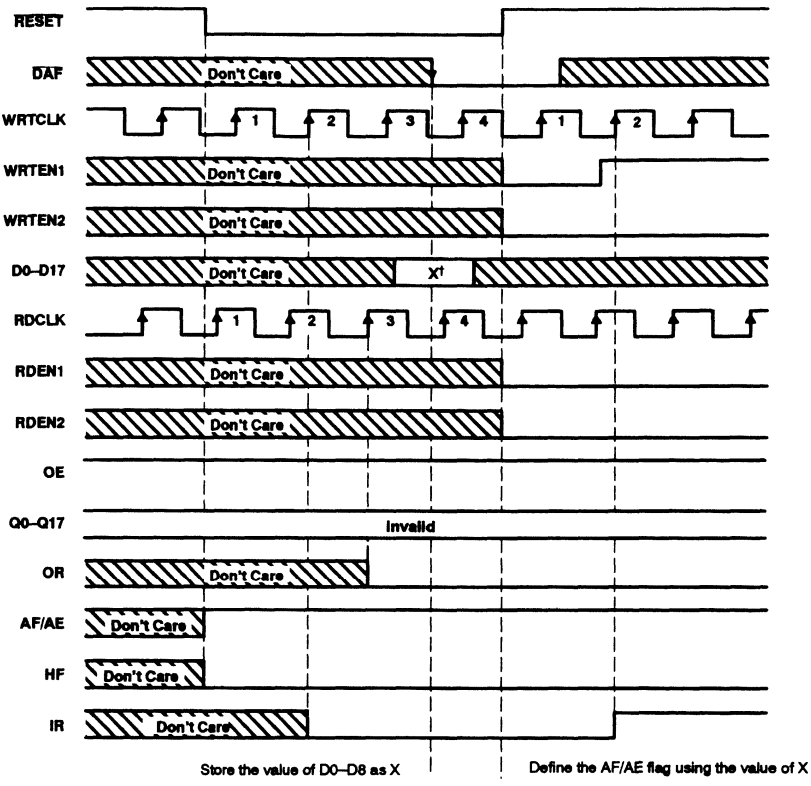
***user-defined X:***

Step 1. Take $\overline{\text{DAF}}$ from high to low.
Step 2. If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low.
Step 3. With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE flag using X.
Step 4. To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low.

***default X:***

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.

## timing diagrams




† X is the binary value of D0–D8 only.

**Figure 1. Reset Cycle: Define AF/AE Using the Value of X**

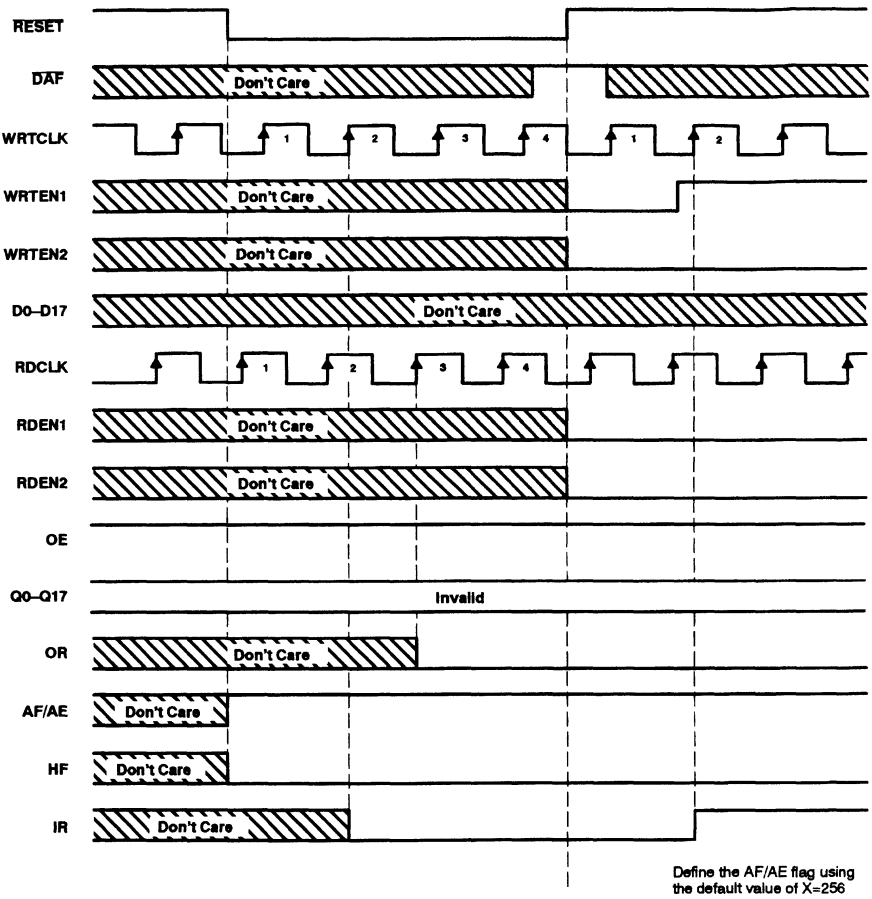



**Figure 2. Reset Cycle: Define AF/AE Using the Default Value**

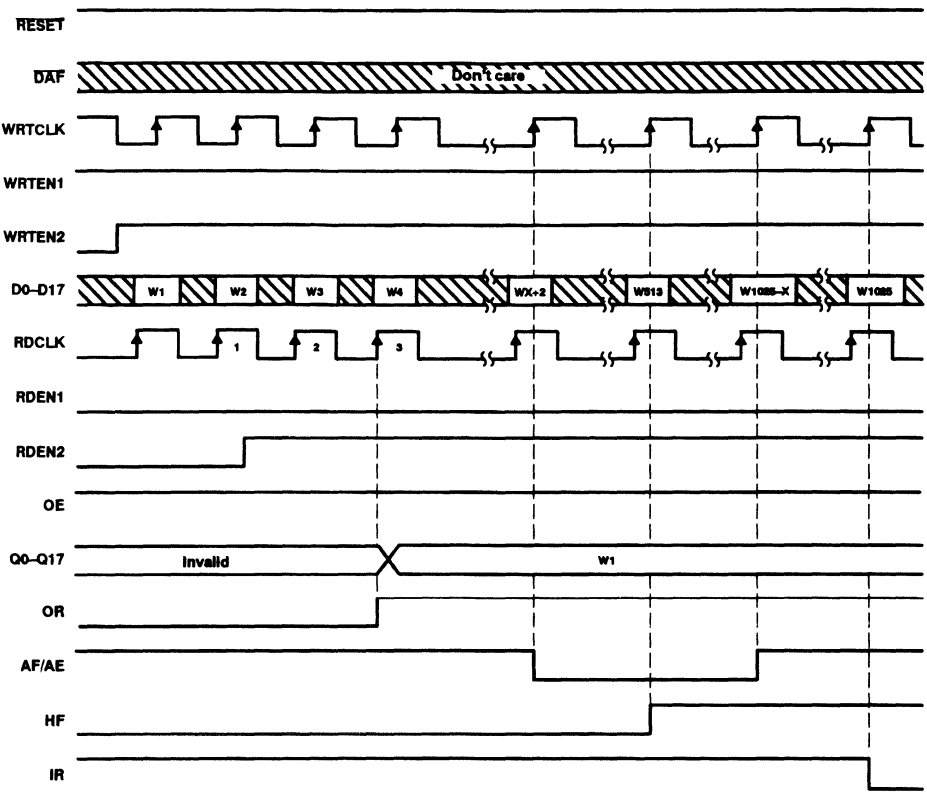



**Figure 3. Write**

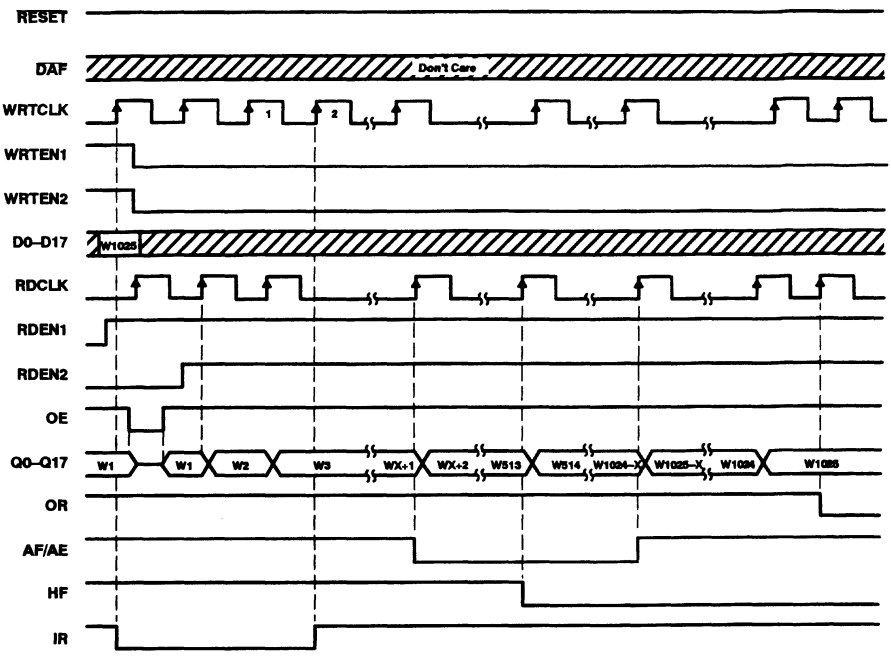



**Figure 4. Read**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | 'ACT7801-15 | | 'ACT7801-18 | | 'ACT7801-20 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | | | 16 | | 16 | | 16 | mA |
| $f_{clock}$ | Clock frequency | | 40 | | 35 | | 28.5 | | MHz |
| $t_w$ | Pulse duration | Data in (D0–D17) high or low | 10 | | 12 | | 14 | | ns |
| | | WRTCLK high | 7 | | 8.5 | | 10 | | |
| | | WRTCLK low | 15 | | 15 | | 15 | | |
| | | RDCLK high | 7 | | 8.5 | | 10 | | |
| | | RDCLK low | 15 | | 15 | | 15 | | |
| | | $\overline{DAF}$ high | 10 | | 10 | | 10 | | |
| | | WRTEN1, WRTEN2 high or low | 10 | | 10 | | 10 | | |
| | | OE, RDEN1, RDEN2 high or low | 10 | | 10 | | 10 | | |
| $t_{su}$ | Setup time | Data in (D0–D17) before WRTCLK↑ | 5 | | 5 | | 5 | | ns |
| | | WRTEN1, WRTEN2 before WRTCLK↑ | 5 | | 5 | | 5 | | |
| | | OE, RDEN1, RDEN2 before RDCLK↑ | 5 | | 5 | | 5 | | |
| | | Reset: $\overline{RESET}$ low before first WRTCLK and RDCLK↑ | 7 | | 7 | | 7 | | |
| | | Define AF/AE: D0–D8 before $\overline{DAF}$↓ | 5 | | 5 | | 5 | | |
| | | Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑ | 7 | | 7 | | 7 | | |
| | | Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑ | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time | Data in (D0–D17) after WRTCLK↑ | 1 | | 1 | | 1 | | ns |
| | | WRTEN1, WRTEN2 after WRTCLK↑ | 1 | | 1 | | 1 | | |
| | | OE, RDEN1, RDEN2 after RDCLK↑ | 1 | | 1 | | 1 | | |
| | | Reset: $\overline{RESET}$ low after fourth WRTCLK and RDCLK↑ | 0 | | 0 | | 0 | | |
| | | Define AF/AE: D0–D8 after $\overline{DAF}$↓ | 1 | | 1 | | 1 | | |
| | | Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑ | 0 | | 0 | | 0 | | |
| | | Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑ | 1 | | 1 | | 1 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 8 mA | 2.4 | | | V |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC1}$‡ | Supply current | $f_{clock}$ = 25 MHz§ | | | 200 | 230 | mA |
| $I_{CC2}$‡ | Standby current | $V_{IH}$ = WRTCLK, | $V_I$ = $V_{IH}$ or $V_{IL}$ | | 20 | 25 | mA |
| $I_{CC3}$‡ | Power-down current | $V_I$ = $V_{CC}$ – 0.2 V or 0 | | | | 400 | μA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (see Figures 9 and 10)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7801-15 | | | 'ACT7801-18 | | 'ACT7801-20 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | WRTCLK or RDCLK | | 40 | | | 35 | | 28.5 | | MHz |
| $t_{pd}$ | RDCLK↑ | Any Q | 5 | 12 | 15 | 5 | 18 | 5 | 20 | ns |
| $t_{pd}$¶ | | | | 10.5 | | | | | | |
| $t_{pd}$ | WRTCLK↑ | IR | 4 | | 10 | 4 | 12 | 4 | 14 | ns |
| $t_{pd}$ | RDCLK↑ | OR | 4 | | 10 | 4 | 12 | 4 | 14 | ns |
| $t_{pd}$ | WRTCLK↑ | AF/AE | 7 | | 20 | 7 | 22 | 7 | 24 | ns |
| $t_{pd}$ | RDCLK↑ | AF/AE | 7 | | 20 | 7 | 22 | 7 | 24 | ns |
| $t_{PLH}$ | WRTCLK↑ | HF | 6 | | 19 | 6 | 21 | 6 | 23 | ns |
| $t_{PHL}$ | RDCLK↑ | | 6 | | 19 | 6 | 21 | 6 | 23 | |
| $t_{PLH}$ | RESET↓ | AF/AE | 4 | | 19 | 4 | 21 | 4 | 23 | ns |
| $t_{PHL}$ | | HF | 4 | | 21 | 4 | 23 | 4 | 25 | |
| $t_{en}$ | OE | Any Q, OR | 4 | | 11 | 4 | 11 | 4 | 11 | ns |
| $t_{dis}$ | | | 2 | | 14 | 2 | 14 | 2 | 14 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ $I_{CC}$ tested with outputs open.
§ For frequencies greater than 25 MHz, $I_{CC}$ = 230 mA + (6 mA × [f – 25 MHz]).
¶ This parameter is measured with $C_L$ = 30 pF (see Figure 5).

## TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

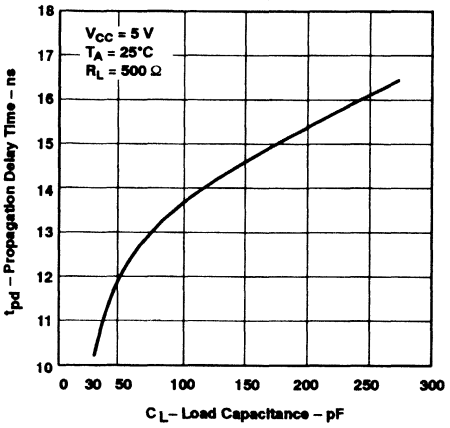



Figure 5

TYPICAL POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

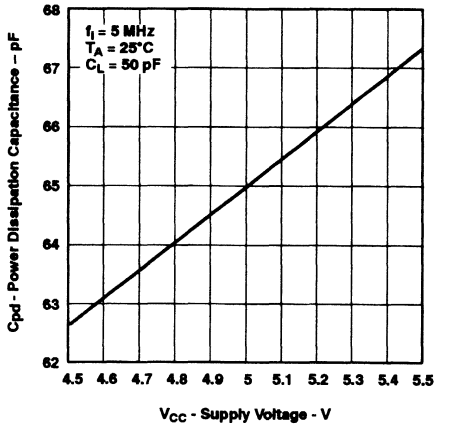



Figure 6

### calculating power dissipation

With $I_{CCF}$ taken from Figure 6, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_{pd} \times V_{CC}^2 \times fi) + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta\ I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## APPLICATION DATA

### expanding the SN74ACT7801

The SN74ACT7801 is expandable in width and depth. Expanding in word depth offers special timing considerations:

1. After the first data word is loaded into the FIFO, the word is unloaded, and the output ready flag output (OR) goes high after (N × 3) read clock (RDCLK) cycles, where N is the number of devices used in depth expansion.
2. After the FIFO is filled, the input ready flag output (IR) goes low, the first word is unloaded, and the IR flag output is driven high after (N × 2) write clock cycles, where N is the number of devices used in depth expansion.

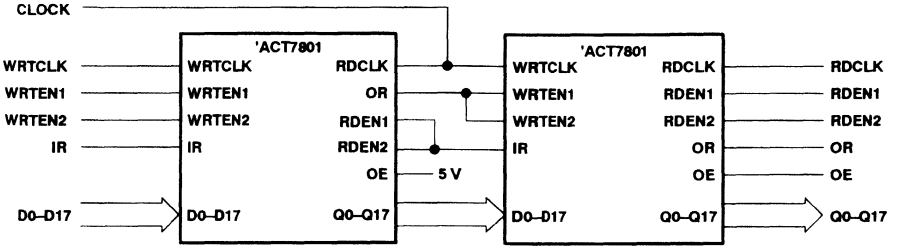



**Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2**

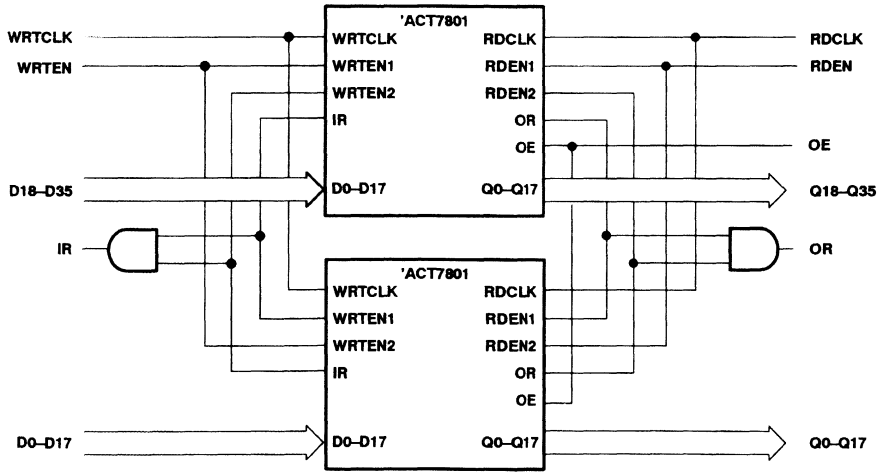



**Figure 8. Word-Width Expansion: 1024 Words × 36 Bits**

## PARAMETER MEASUREMENT INFORMATION

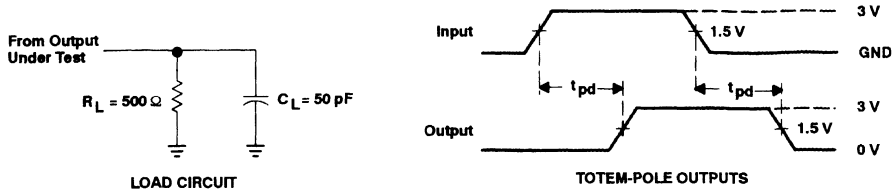
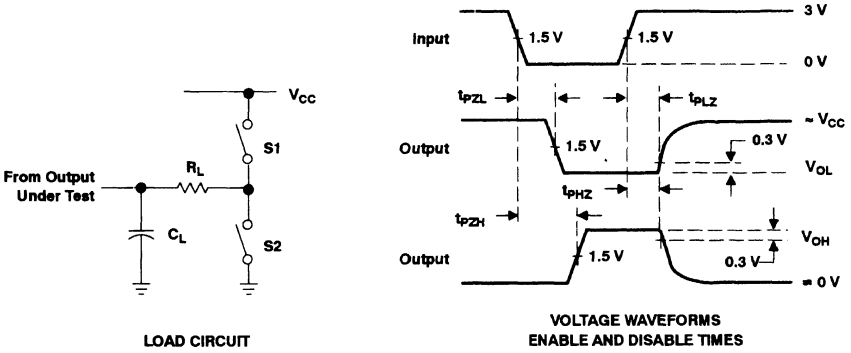



**Figure 9. Standard CMOS Outputs (OR, Half Full, AF/AE)**




| PARAMETER | | $R_L$ | $C_L$† | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | – | 50 pF | Open | Open |

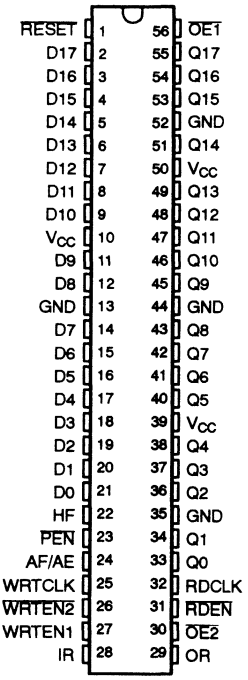
† Includes probe and test fixture capacitance.

**Figure 10. 3-State Outputs (Any Q, OR)**

SCAS191–D3993, MARCH 1991–REVISED MARCH 1992

- **Member of the Texas Instruments *Widebus*™ Family**
- **Free-Running Read and Write Clocks May Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**
- **512 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost Full/Almost Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7805 and SN74ACT7813**

DL PACKAGE
(TOP VIEW)




## description

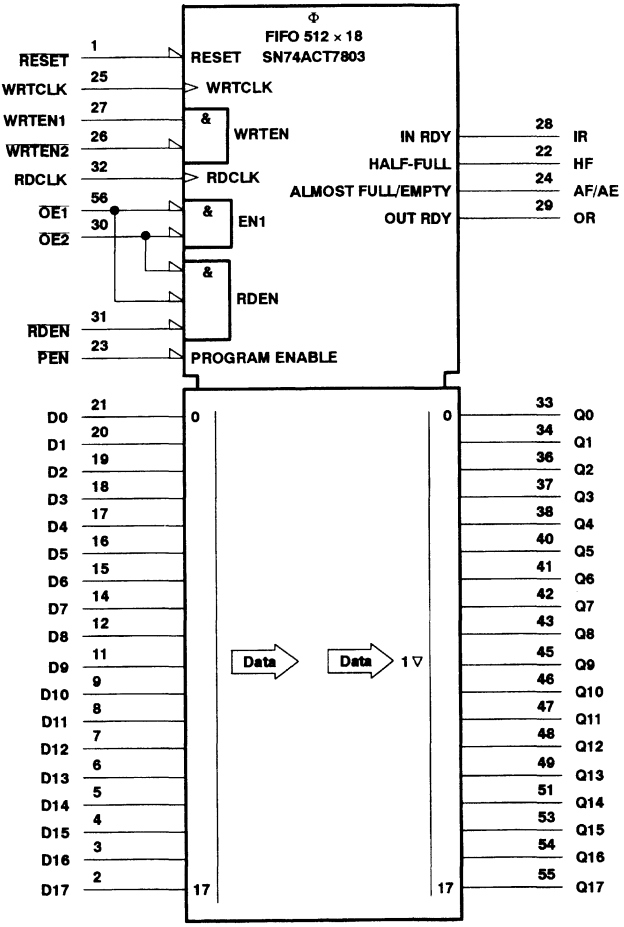
The SN74ACT7803 is a 512-word × 18-bit FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices may be configured for bidirectional data buffering without additional logic. Multiple distributed $V_{CC}$ and GND pins along with TI's patented Output Edge Control (OEC™) circuit dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) should be free-running and may be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO may be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

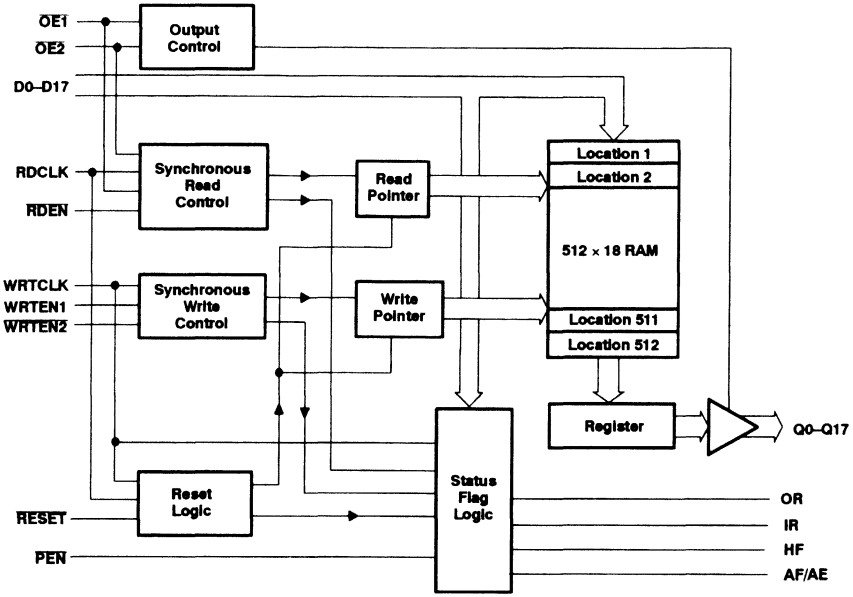
Widebus and OEC are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

## functional block diagram



## Terminal Functions

| PIN NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AF/AE | 24 | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 64 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (512 minus Y) or more words. AF/AE is high after reset. |
| D0–D17 | 21–14, 12–11, 9–2 | I | 18-bit data input port |
| HF | 22 | O | Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset. |
| IR | 28 | O | Input ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset. |
| $\overline{OE1}$, $\overline{OE2}$ | 56, 30 | I | Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled, and the data outputs are in the high-impedance state. |
| OR | 29 | O | Output ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory. |
| $\overline{PEN}$ | 23 | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high. |
| Q0–Q17 | 33–34, 36–38, 40–43, 45–49, 51, 53–55 | O | 18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17. |
| RDCLK | 32 | I | Read clock. RDCLK is a continuous clock and may be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition of RDCLK. |
| $\overline{RDEN}$ | 31 | I | Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK. |
| $\overline{RESET}$ | 1 | I | Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high. |
| WRTCLK | 25 | I | Write clock. WRTCLK is a continuous clock and may be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK. |
| WRTEN1, $\overline{WRTEN2}$ | 27, 26 | I | Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK. |

## timing diagram

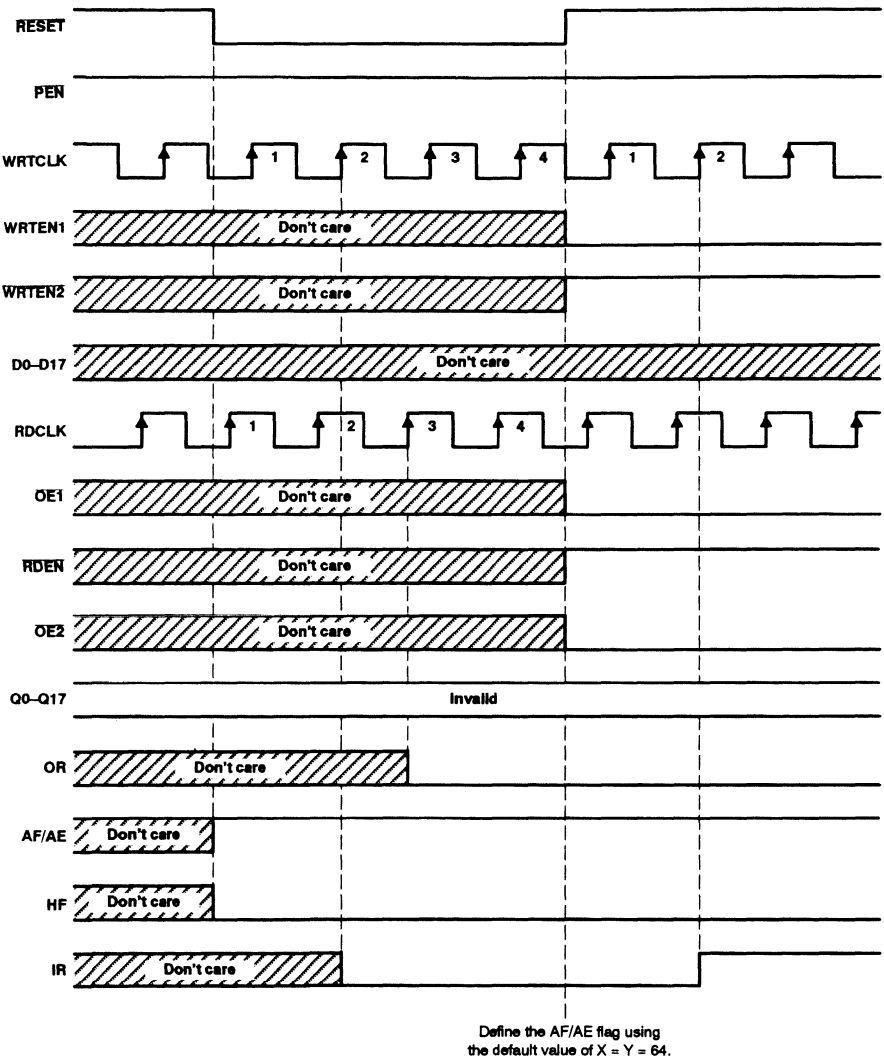



**Figure 1. Reset Cycle**

## timing diagram

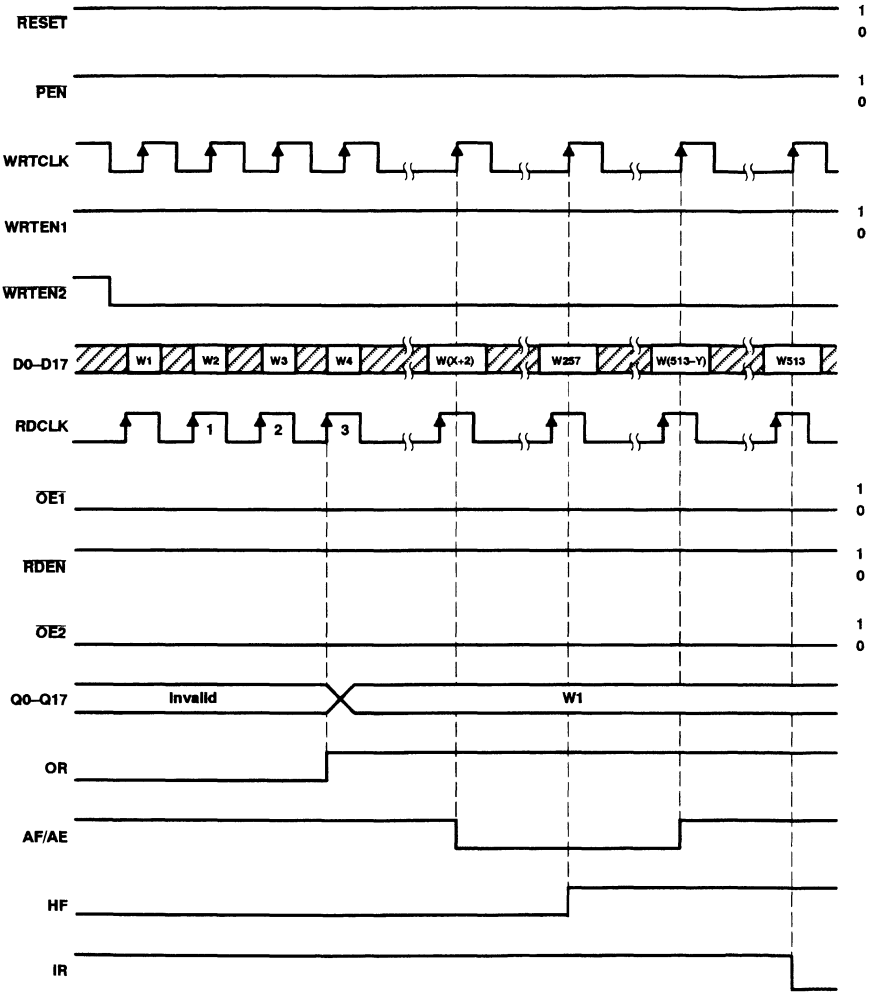



Figure 2. Write

## timing diagram

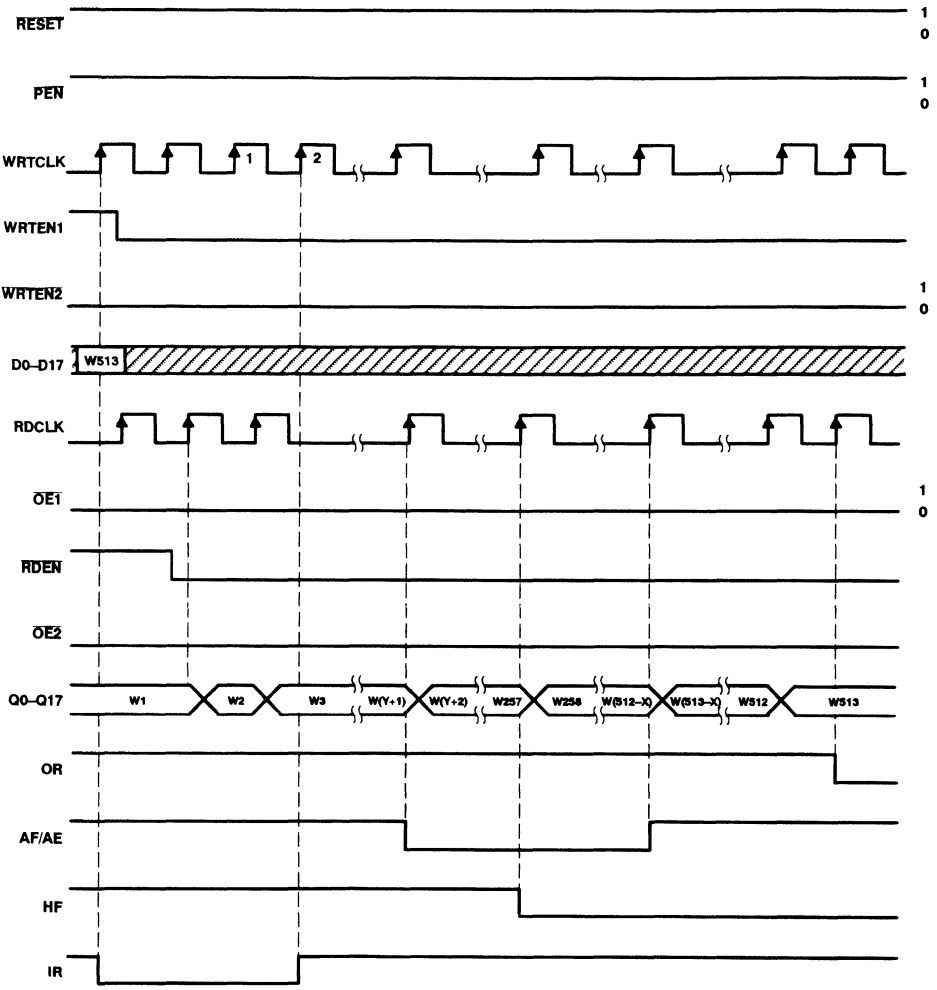



**Figure 3. Read**

### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost empty offset value (X) and the almost full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 64 are used. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ may be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK will reprogram Y to the binary value on D0–D7 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{WRTEN2}$). A maximum value of 255 may be programmed for either X or Y. To use the default values of X = Y = 64, $\overline{PEN}$ must be held high.

### timing diagram

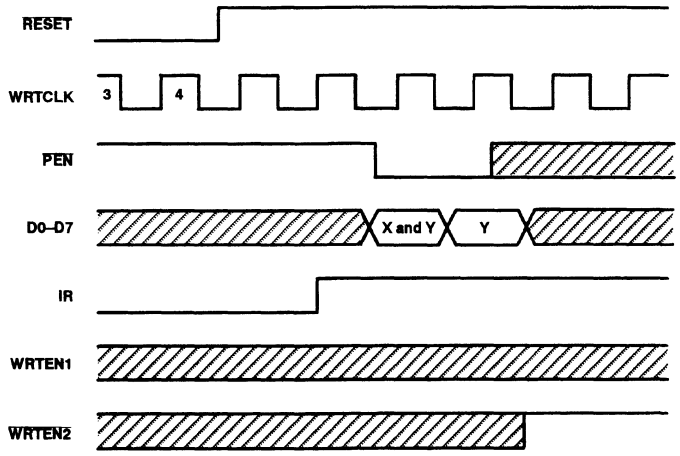



**Figure 4. Programming X and Y Separately**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage, $V_I$ | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | 'ACT7803-15 | | 'ACT7803-20 | | 'ACT7803-25 | | 'ACT7803-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 67 | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | WRTCLK high or low | 6 | | 7 | | 8 | | 12 | | ns |
| | | RDCLK high or low | 6 | | 7 | | 8 | | 12 | | |
| | | $\overline{PEN}$ low | 8 | | 9 | | 9 | | 12 | | |
| $t_{su}$ | Setup time | Data in (D0–D17) before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | ns |
| | | WRTEN1, $\overline{WRTEN2}$ before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| | | $\overline{OE1}$, $\overline{OE2}$ before RDCLK↑ | 5 | | 5 | | 6 | | 6 | | |
| | | $\overline{RDEN}$ before RDCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| | | Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑† | 5 | | 6 | | 6 | | 6 | | |
| | | $\overline{PEN}$ before WRTCLK↑ | 5 | | 6 | | 6 | | 6 | | |
| $t_h$ | Hold time | Data in (D0–D17) after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | ns |
| | | WRTEN1, $\overline{WRTEN2}$ after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | $\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑† | 2 | | 2 | | 2 | | 2 | | |
| | | $\overline{PEN}$ high after WRTCLK↓ | 0 | | 0 | | 0 | | 0 | | |
| | | $\overline{PEN}$ low after WRTCLK↑ | 2 | | 2 | | 2 | | 2 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

† To permit the clock pulse to be utilized for reset purposes.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$‡ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 9 and 10)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7803-15 | | | 'ACT7803-20 | | 'ACT7803-25 | | 'ACT7803-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | WRTCLK or RDCLK | | 67 | | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | RDCLK↑ | Any Q | 4 | 9.5 | 12 | 4 | 13 | 4 | 15 | 4 | 20 | ns |
| $t_{pd}$§ | | | | 8.5 | | | | | | | | |
| $t_{pd}$ | WRTCLK↑ | IR | 3 | | 8.5 | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | RDCLK↑ | OR | 3 | | 8.5 | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | WRTCLK↑ | AF/AE | 7 | | 16.5 | 7 | 19 | 7 | 21 | 7 | 23 | ns |
| $t_{pd}$ | RDCLK↑ | AF/AE | 7 | | 17 | 7 | 19 | 7 | 21 | 7 | 23 | ns |
| $t_{PLH}$ | WRTCLK↑ | HF | 7 | | 15 | 7 | 17 | 7 | 19 | 7 | 21 | ns |
| $t_{PHL}$ | RDCLK↑ | | 7 | | 15.5 | 7 | 18 | 7 | 20 | 7 | 22 | |
| $t_{PLH}$ | $\overline{RESET}$ low | AF/AE | 2 | | 9 | 2 | 11 | 2 | 13 | 2 | 15 | ns |
| $t_{PHL}$ | | HF | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | |
| $t_{en}$ | $\overline{OE1}$, $\overline{OE2}$ | Any Q | 2 | | 8.5 | 2 | 11 | 2 | 11 | 2 | 11 | ns |
| $t_{dis}$ | | | 2 | | 9.5 | 2 | 11 | 2 | 14 | 2 | 14 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

§ This parameter is measured with a 30 pF load (see Figure 7).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | 53 | pF |

## APPLICATION INFORMATION

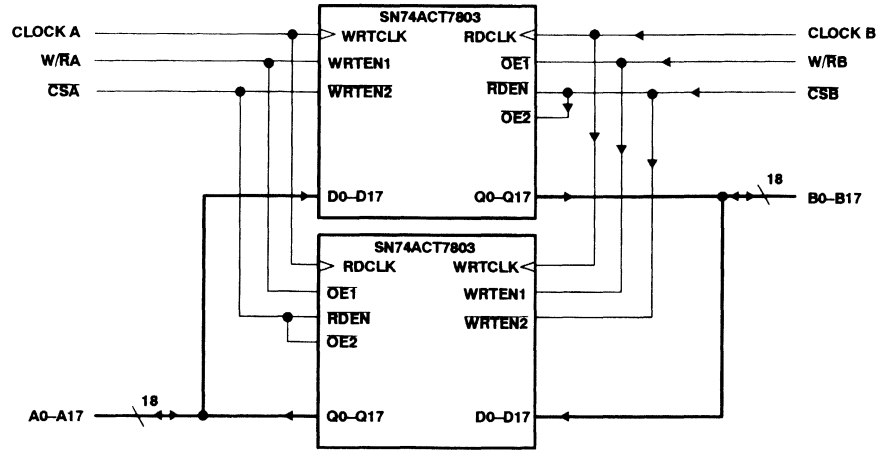



**Figure 5. Bidirectional Configuration**

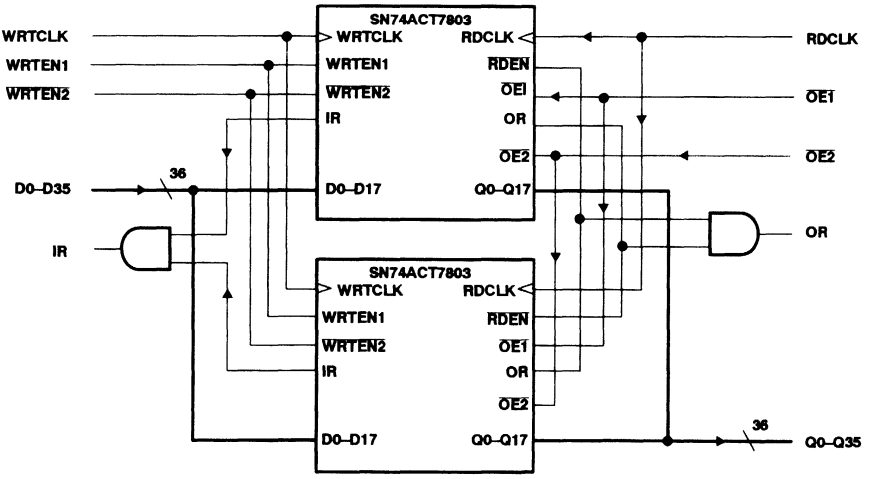



**Figure 6. Word-Width Expansion: 512 × 36 Bit**

## TYPICAL CHARACTERISTICS

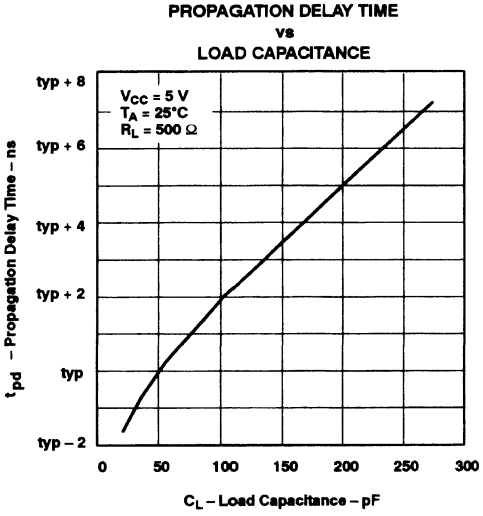



Figure 7

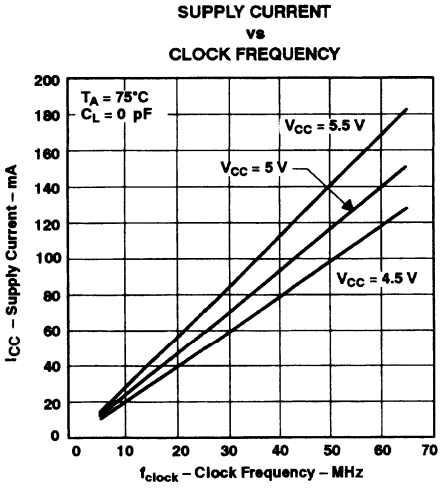



Figure 8



TEXAS INSTRUMENTS

### calculating power dissipation

With $I_{CCF}$ taken from Figure 8, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

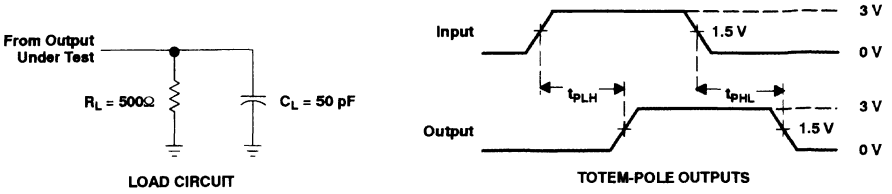
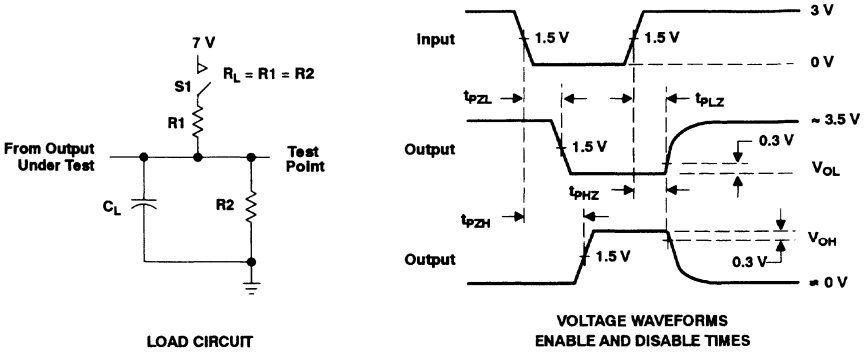



**Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)**




| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

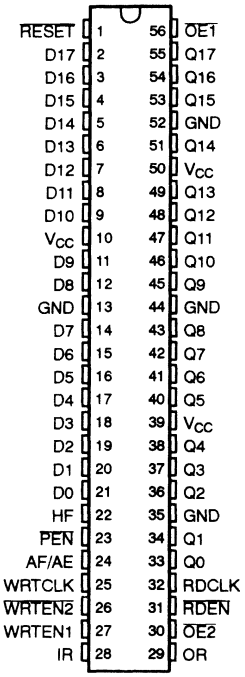
† Includes probe and test fixture capacitance.

**Figure 10. 3-State Outputs (Any Q)**

SCAS201–D4007, MARCH 1991–REVISED APRIL 1992

- **Member of the Texas Instruments *Widebus* ™ Family**
- **Free-Running Read and Write Clocks May Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**
- **256 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost Full/Almost Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7803 and SN74ACT7813**

DL PACKAGE
(TOP VIEW)




## description

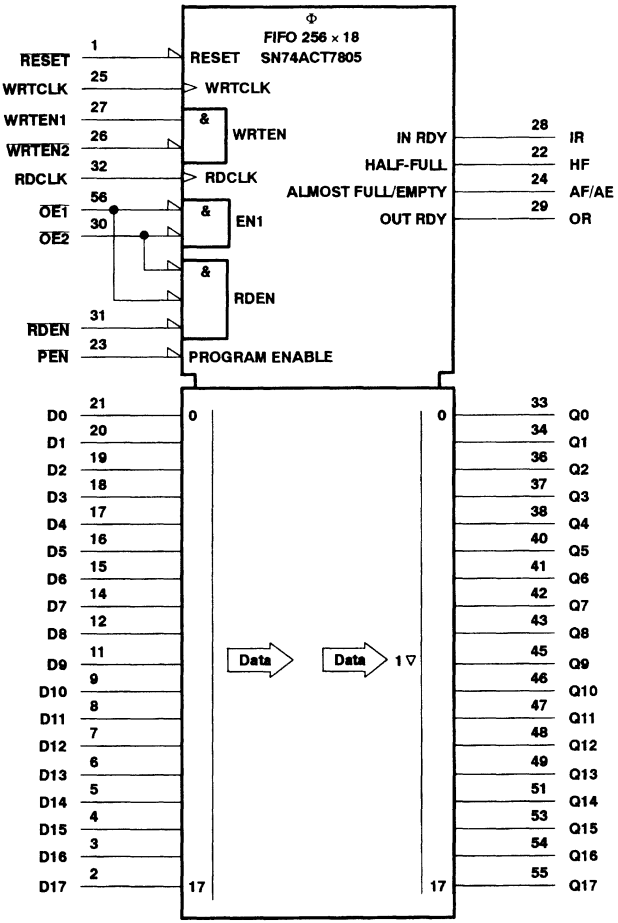
The SN74ACT7805 is a 256-word × 18-bit clocked FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices may be configured for bidirectional data buffering without additional logic. Multiple distributed $V_{CC}$ and GND pins along with TI's patented Output Edge Control (OEC™) circuit dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) should be free-running and may be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO may be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

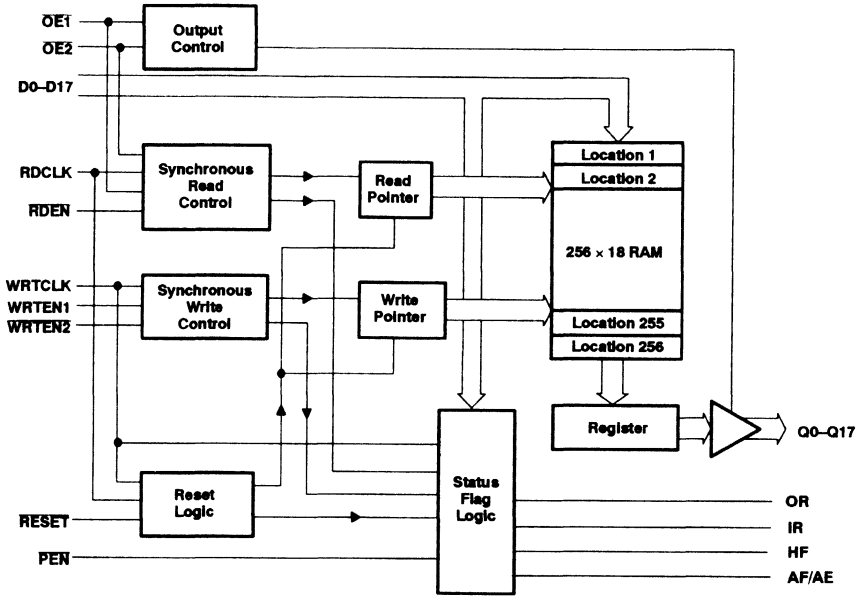
Widebus and OEC are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

## functional block diagram



## Terminal Functions

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AF/AE | 24 | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 32 may be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (256 minus Y) or more words. AF/AE is high after reset. |
| D0–D17 | 21–14, 12–11, 9–2 | I | 18-bit data input port |
| HF | 22 | O | Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset. |
| IR | 28 | O | Input ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset. |
| $\overline{OE1}$, $\overline{OE2}$ | 56, 30 | I | Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled, and the data outputs are in the high-impedance state. |
| OR | 29 | O | Output ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory. |
| $\overline{PEN}$ | 23 | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high. |
| Q0–Q17 | 33–34, 36–38, 40–43, 45–49, 51, 53–55 | O | 18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17. |
| RDCLK | 32 | I | Read clock. RDCLK is a continuous clock and may be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK. |
| $\overline{RDEN}$ | 31 | I | Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK. |
| $\overline{RESET}$ | 1 | I | Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high. |
| WRTCLK | 25 | I | Write clock. WRTCLK is a continuous clock and may be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK. |
| WRTEN1, $\overline{WRTEN2}$ | 27, 26 | I | Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK. |

## timing diagrams

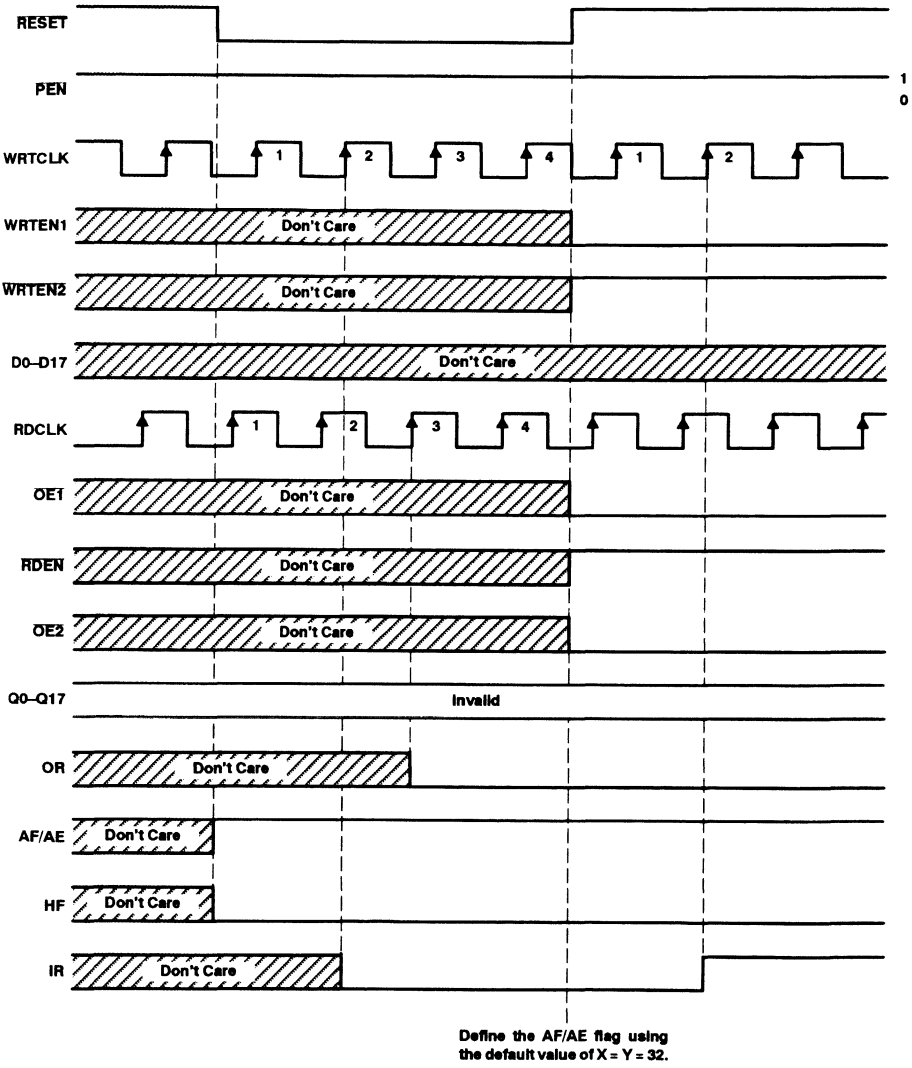



Figure 1. Reset Cycle

## timing diagrams (continued)

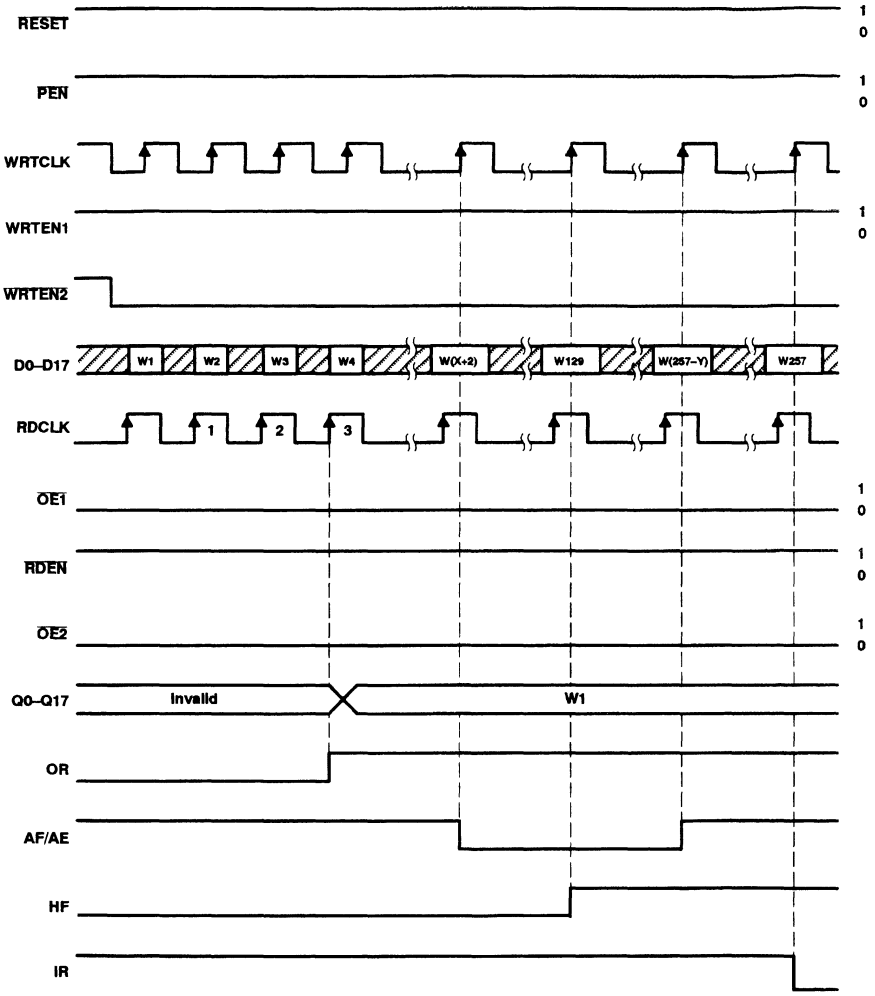



Figure 2. Write

**timing diagrams (continued)**

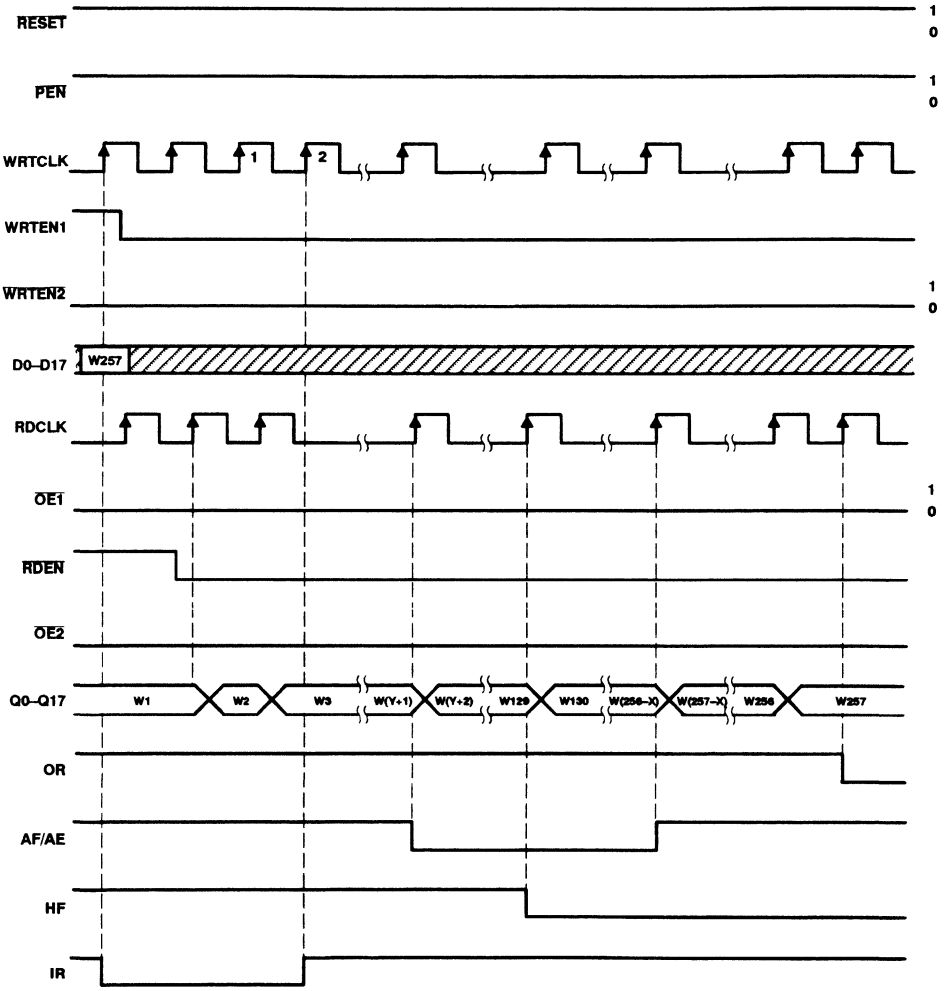



**Figure 3. Read**

### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost empty offset value (X) and the almost full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 32 are used. The AF/AE flag is high when the FIFO contains X or less words or (256 minus Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ may be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D6 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK will reprogram Y to the binary value on D0–D6 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{WRTEN2}$). A maximum value of 127 may be programmed for either X or Y. To use the default values of X = Y = 32, $\overline{PEN}$ must be held high.

### timing diagram

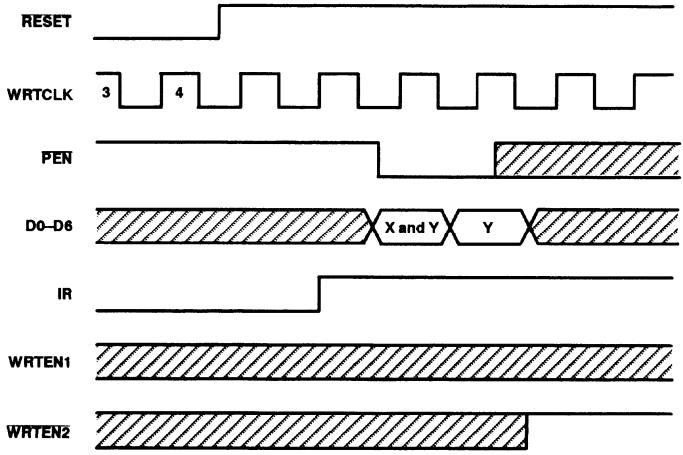



**Figure 4. Programming X and Y Separately**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | 'ACT7805-15 | | 'ACT7805-20 | | 'ACT7805-25 | | 'ACT7805-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 67 | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | WRTCLK high or low | 6 | | 7 | | 8 | | 12 | | ns |
| | | RDCLK high or low | 6 | | 7 | | 8 | | 12 | | |
| | | $\overline{PEN}$ low | 8 | | 9 | | 9 | | 12 | | |
| $t_{su}$ | Setup time | Data in (D0–D17) before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | ns |
| | | WRTEN1, $\overline{WRTEN2}$ before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| | | $\overline{OE1}$, $\overline{OE2}$ before RDCLK↑ | 5 | | 5 | | 6 | | 6 | | |
| | | $\overline{RDEN}$ before RDCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| | | Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑† | 5 | | 6 | | 6 | | 6 | | |
| | | WRTCLK low before $\overline{PEN}$↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE: $\overline{PEN}$ before WRTCLK↑ | 5 | | 6 | | 6 | | 6 | | |
| $t_h$ | Hold time | Data in (D0–D17) after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | ns |
| | | WRTEN1, $\overline{WRTEN2}$ after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | $\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑† | 2 | | 2 | | 2 | | 2 | | |
| | | Define AF/AE: $\overline{PEN}$ after WRTCLK↑ | 2 | | 2 | | 2 | | 2 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

† To permit the clock pulse to be utilized for reset purposes.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ – 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$‡ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 9 and 10)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7805-15 | | | 'ACT7805-20 | | 'ACT7805-25 | | 'ACT7805-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | WRTCLK or RDCLK | | 67 | | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | RDCLK↑ | Any Q | 4 | 9.5 | 12 | 4 | 13 | 4 | 15 | 4 | 20 | ns |
| $t_{pd}$§ | | | | 8.5 | | | | | | | | |
| $t_{pd}$ | WRTCLK↑ | IR | 3 | | 8.5 | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | RDCLK↑ | OR | 3 | | 8.5 | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | WRTCLK↑ | AF/AE | 7 | | 16.5 | 7 | 19 | 7 | 21 | 7 | 23 | ns |
| $t_{pd}$ | RDCLK↑ | | 7 | | 17 | 7 | 19 | 7 | 21 | 7 | 23 | |
| $t_{PLH}$ | WRTCLK↑ | HF | 7 | | 15 | 7 | 17 | 7 | 19 | - | 21 | ns |
| $t_{PHL}$ | RDCLK↑ | | 7 | | 15.5 | 7 | 18 | 7 | 20 | 7 | 22 | |
| $t_{PLH}$ | $\overline{RESET}$ low | AF/AE | 2 | | 9 | 2 | 11 | 2 | 13 | 2 | 15 | ns |
| $t_{PHL}$ | | HF | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | |
| $t_{en}$ | $\overline{OE1}$, $\overline{OE2}$ | Any Q | 2 | | 8.5 | 2 | 11 | 2 | 11 | 2 | 11 | ns |
| $t_{dis}$ | | | 2 | | 9.5 | 2 | 11 | 2 | 14 | 2 | 14 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.
§ This parameter is measured at $C_L$ = 30 pF load (see Figure 7).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per FIFO channel | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | 53 | pF |

## APPLICATION INFORMATION

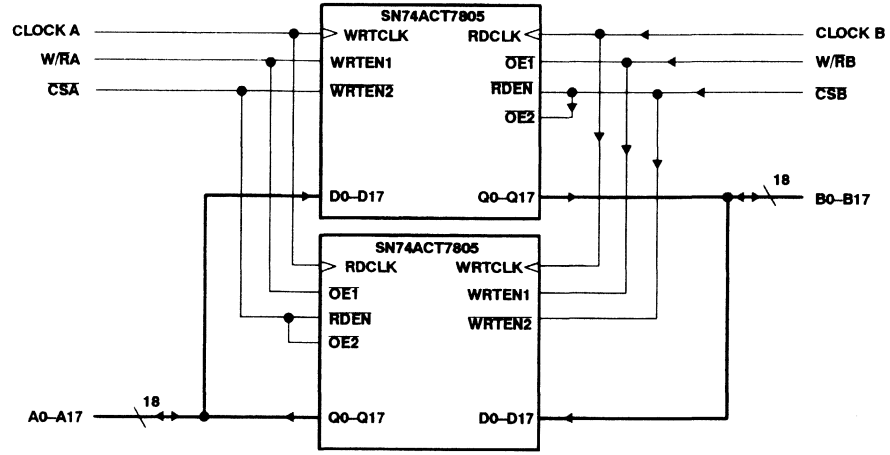



**Figure 5. Bidirectional Configuration**

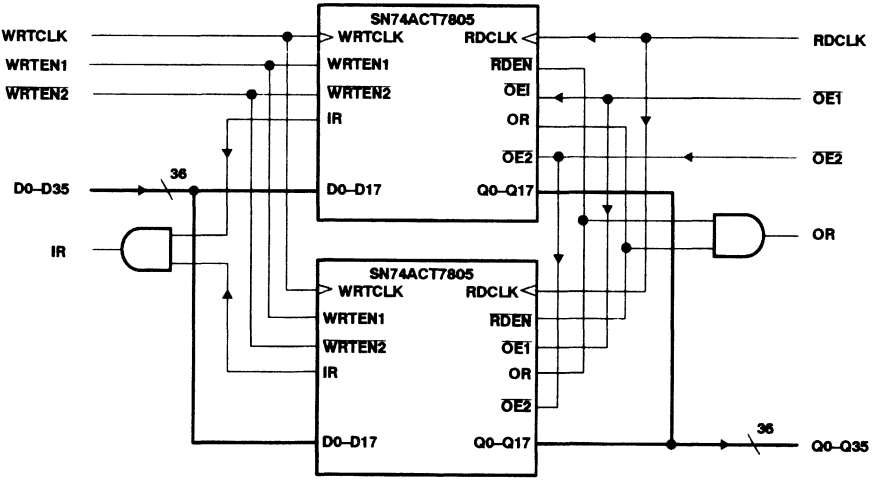



**Figure 6. Word-Width Expansion: 256 × 36 Bits**

## TYPICAL CHARACTERISTICS

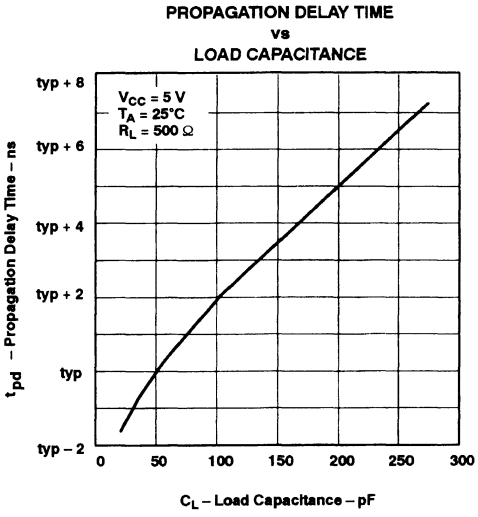



Figure 7

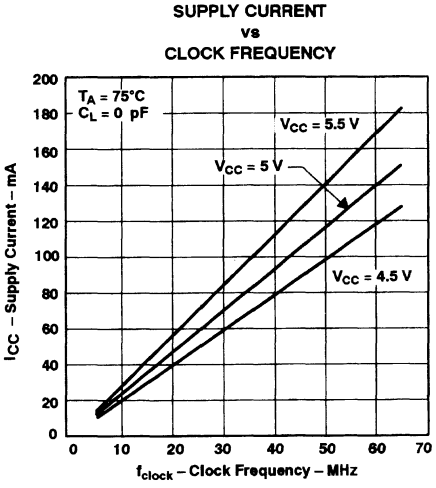



Figure 8



TEXAS INSTRUMENTS

### calculating power dissipation

With $I_{CCF}$ taken from Figure 8, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_{pd} \times V_{CC}^2 \times fi) + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta\ I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

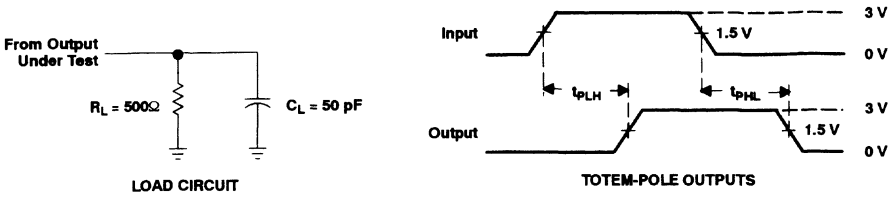
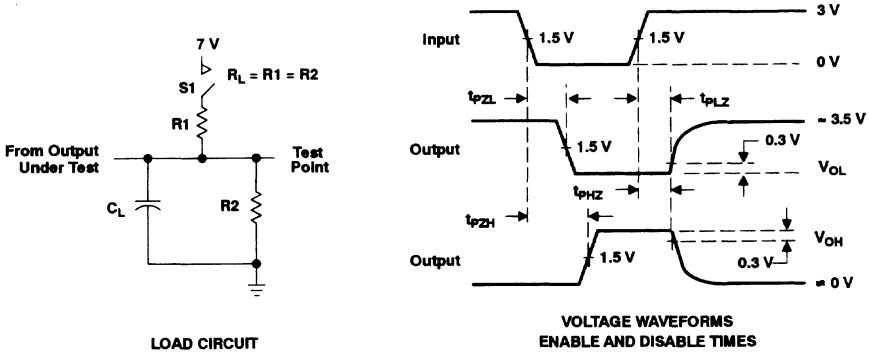



**Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)**




| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

† Includes probe and test fixture capacitance.

**Figure 10. 3-State Outputs (Any Q)**

SCAS200–D4005, JANUARY 1991–REVISED APRIL 1992

- **Free-Running Read and Write Clocks May Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Programmable Almost Full/Almost Empty Flag**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable In Word Width and/or Word Depth**
- **Fast Access Times of 12 ns With a 50-pF Load**
- **Data Rates From 0 to 67 MHz**
- **3-State Outputs**
- **Available In 44-Pin PLCC (FN) or Space-Saving 64-Pin Shrink Quad Flat Pack (PM)**

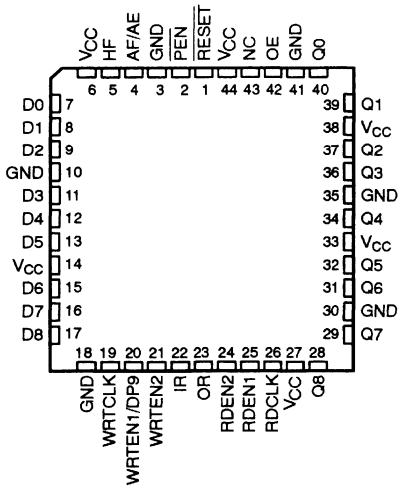
## description

The SN74ACT7807 is a 2048-word by 9-bit FIFO with high speed and fast access times. It processes data at rates up to 67 MHz and access times of 12 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

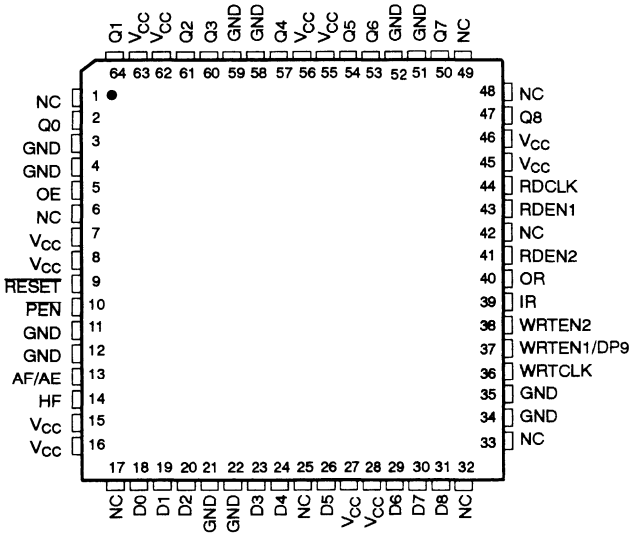
The write clock (WRTCLK) and read clock (RDCLK) inputs should be free-running and may be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when the write-enable (WRTEN1/DP9, WRTEN2) inputs are high and the input-ready (IR) flag output is high. Data is read from memory on the rising edge of RDCLK when the read-enable (RDEN1, RDEN2) and output-enable (OE) inputs are high and the output-ready (OR) flag output is high. The first word written to memory is clocked through to the output buffer regardless of the levels on RDEN1, RDEN2, and OE. The OR flag indicates that valid data is present on the output buffer.

The FIFO may be reset asynchronous to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK cycles occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

**FN PACKAGE**
**(TOP VIEW)**




**PM PACKAGE**
**(TOP VIEW)**

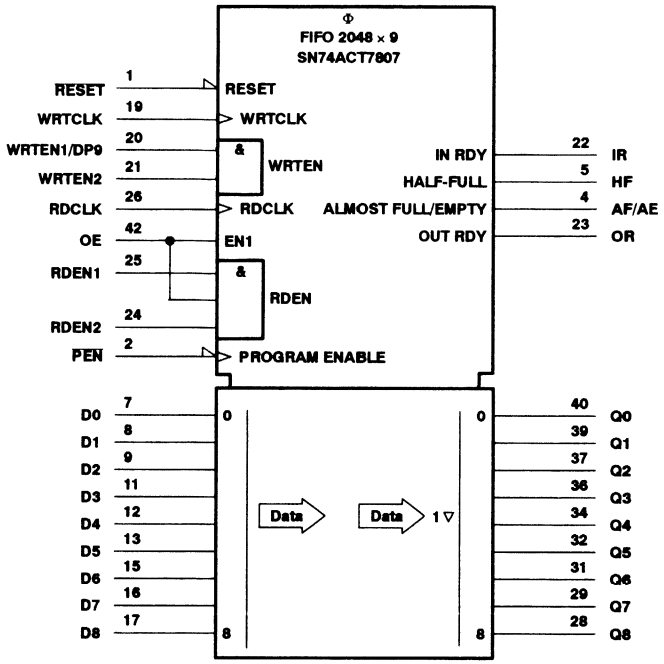



NC – No internal connection



TEXAS INSTRUMENTS

## logic symbol†

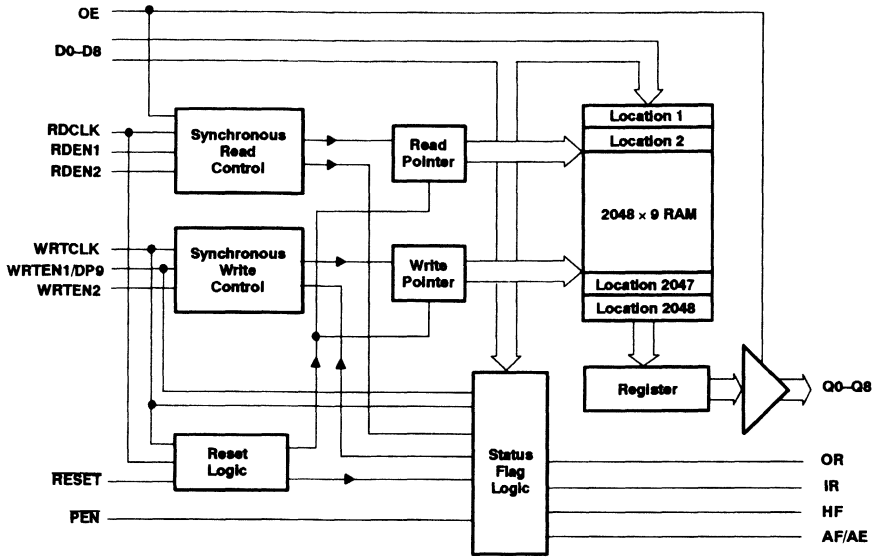



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| AF/AE | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 256 may be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (2048 minus Y) or more words. AF/AE is high after reset. |
| D0–D8 | I | Nine-bit data input port. |
| HF | O | Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset. |
| IR | O | Input ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset. |
| OE | I | Output enable. When OE, RDEN1, RDEN2 and OR are high, data is read from the FIFO on a low-to-high transition of RDCLK. When OE is low, reads are disabled and the data outputs are in the high-impedance state. |
| OR | O | Output ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory. |
| $\overline{PEN}$ | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high. |
| Q0–Q8 | O | Nine-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q8 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q8. |
| RDCLK | I | Read clock. RDCLK is a continuous clock and may be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when RDEN1, RDEN2, OE, and OR are high. OR is synchronous to the low-to-high transition or RDCLK. |
| RDEN1, RDEN2 | I | Read enables. When RDEN1, RDEN2, OE, and OR are high, data is read from the FIFO on the low-to-high transition of RDCLK. |
| $\overline{RESET}$ | I | Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high. |
| WRTCLK | I | Write clock. WRTCLK is a continuous clock and may be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when WRTEN1/DP9, WRTEN2, and IR are high. IR is synchronous to the low-to-high transition of WRTCLK. |
| WRTEN1/DP9 | I | Write enable/data pin 9. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. When programming an AF/AE offset value, WRTEN1/DP9 is used as the most significant data bit. |
| WRTEN2 | I | Write enable. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. |

## functional block diagram



### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost-empty offset value (X) and the almost-full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or less words or (2048 minus Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ may be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D8 and WRTEN1/DP9 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D8 and WRTEN1/DP9 at the time of the second WRTCLK low-to-high transition. While the offsets are programmed, data is not written to the FIFO memory regardless of the state of the write enables (WRTEN1/DP9, WRTEN2).

A maximum value of 1023 may be programmed for either X or Y. To use the default values of X = Y = 256, $\overline{PEN}$ must be held high.

### timing diagrams

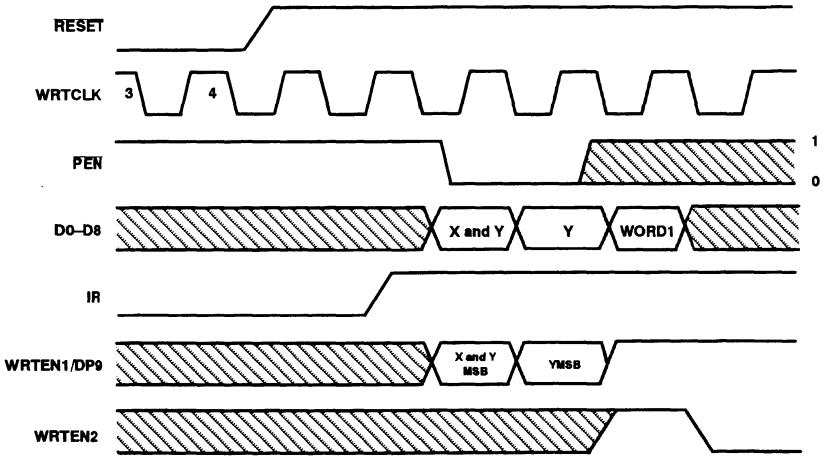



**Figure 1. Programming X and Y Separately**

## timing diagrams (continued)

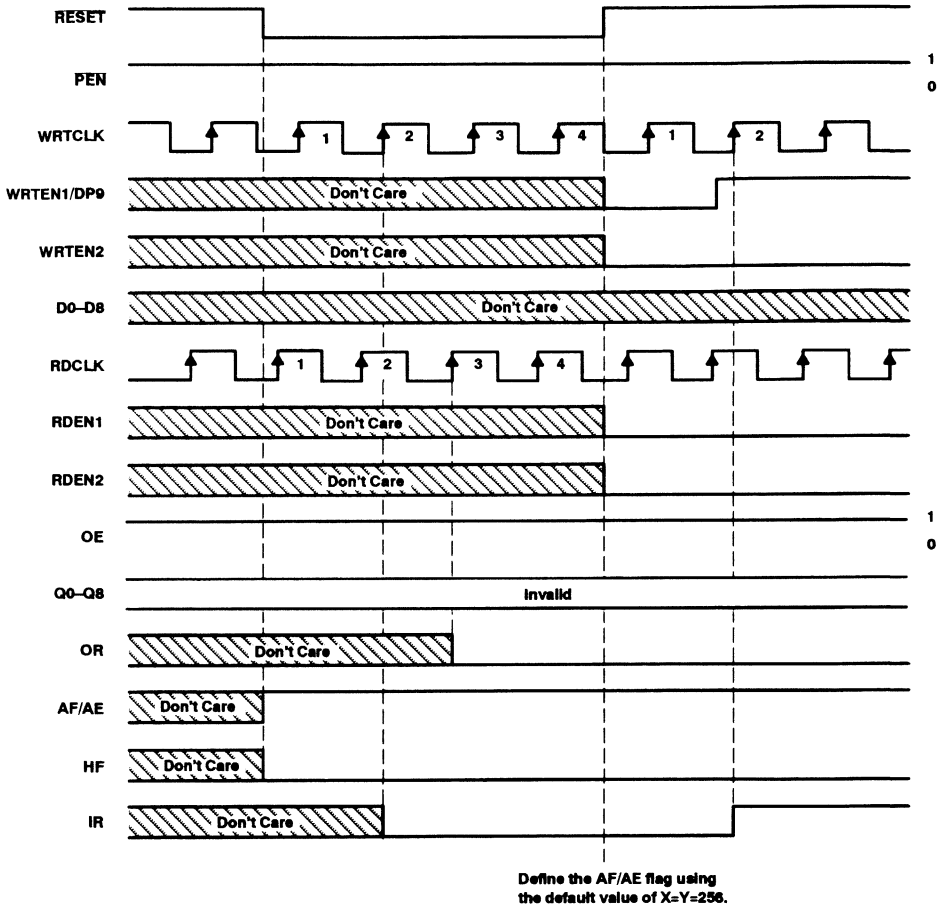



**Figure 2. Reset Cycle: Define AF/AE Using the Default**

## timing diagrams (continued)

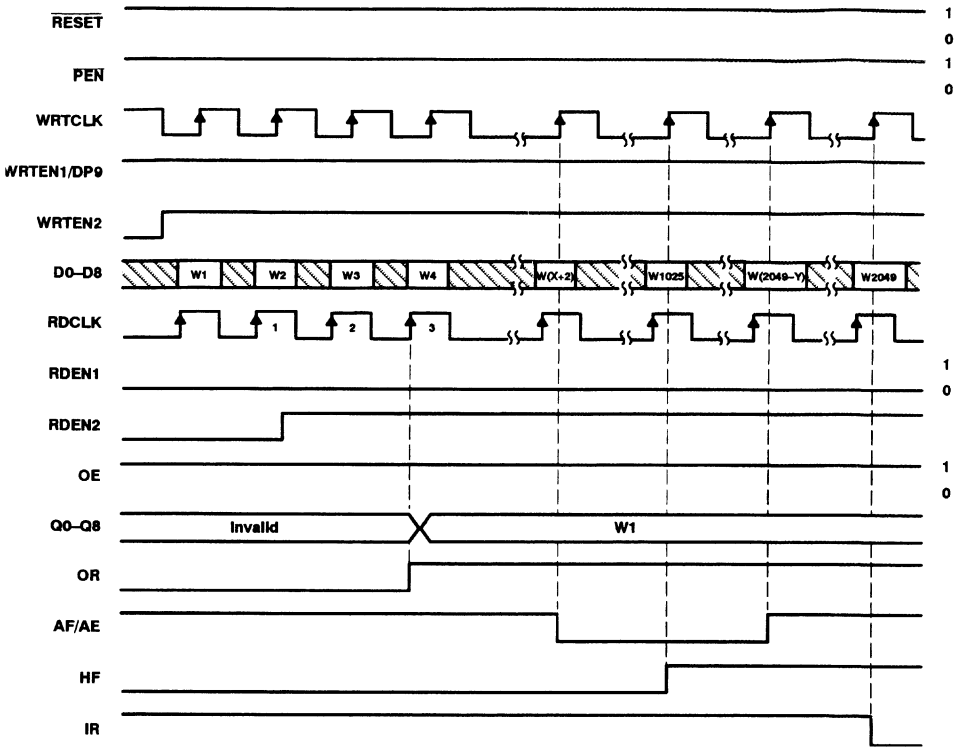



Figure 3. Write

**timing diagrams (continued)**

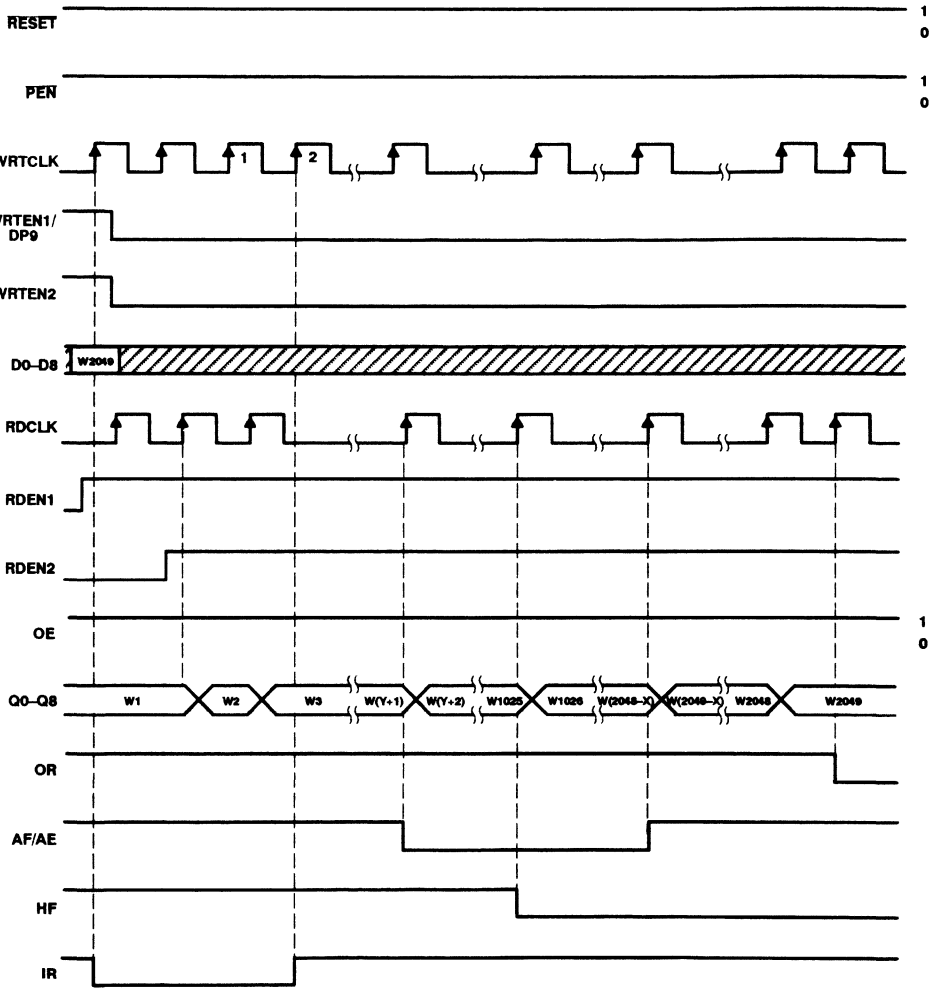



**Figure 4. Read**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | 'ACT7807-15 | | 'ACT7807-20 | | 'ACT7807-25 | | 'ACT7807-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 67 | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | WRTCLK high or low | 6 | | 8 | | 9 | | 13 | | ns |
| | | RDCLK high or low | 6 | | 8 | | 9 | | 13 | | |
| | | $\overline{PEN}$ low | 6 | | 9 | | 9 | | 13 | | |
| $t_{su}$ | Setup time | Data in (D0–D8) before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | ns |
| | | WRTEN1, WRTEN2 before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| | | OE, RDEN1, RDEN2 before RDCLK↑ | 5 | | 6 | | 6 | | 6.5 | | |
| | | Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑† | 7 | | 8 | | 8 | | 8 | | |
| | | $\overline{PEN}$ before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time | Data in (D0–D8) after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | ns |
| | | WRTEN1, WRTEN2 after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | OE, RDEN1, RDEN2 after RDCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑† | 5 | | 5 | | 5 | | 5 | | |
| | | $\overline{PEN}$ high after WRTCLK↓ | 0 | | 0 | | 0 | | 0 | | |
| | | $\overline{PEN}$ low after WRTCLK↑ | 3 | | 3 | | 3 | | 3 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

† To permit the clock pulse to be utilized for reset purposes.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | µA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ – 0.2 V or 0 | | | 400 | µA |
| $\Delta I_{CC}$‡ | WRTEN1/DP9 | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 2 | mA |
| | Other inputs | | | | | 1 | |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 9 and 10)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7807-15 | | | 'ACT7807-20 | | 'ACT7807-25 | | 'ACT7807-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | WRTCLK or RDCLK | | 67 | | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | RDCLK↑ | Any Q | 3 | 9 | 12 | 3 | 13 | 3 | 18 | 3 | 25 | ns |
| $t_{pd}$§ | | | | 8 | | | | | | | | |
| $t_{pd}$ | WRTCLK↑ | IR | 1 | | 9 | 1 | 12 | 1 | 14 | 1 | 16 | ns |
| $t_{pd}$ | RDCLK↑ | OR | 1 | | 9 | 2 | 12 | 2 | 14 | 2 | 16 | ns |
| $t_{pd}$ | WRTCLK↑ | AF/AE | 2 | | 16 | 2 | 20 | 2 | 25 | 2 | 30 | ns |
| $t_{pd}$ | RDCLK↑ | AF/AE | 2 | | 17 | 2 | 20 | 2 | 25 | 2 | 30 | ns |
| $t_{PLH}$ | WRTCLK↑ | HF | 2 | | 19 | 2 | 21 | 2 | 23 | 2 | 25 | ns |
| $t_{PHL}$ | RDCLK↑ | | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | |
| $t_{PLH}$ | RESET low | AF/AE | 1 | | 12 | 1 | 18 | 1 | 22 | 1 | 24 | ns |
| $t_{PHL}$ | | HF | 2 | | 12 | 2 | 18 | 2 | 22 | 2 | 24 | |
| $t_{en}$ | OE | Any Q | 2 | | 10 | 2 | 13 | 2 | 15 | 2 | 18 | ns |
| $t_{dis}$ | | | 1 | | 11 | 1 | 13 | 1 | 15 | 1 | 18 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

§ This parameter is measured with $C_L$ = 30 pF (see Figure 7).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per FIFO channel | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | 91 | pF |

## APPLICATION INFORMATION

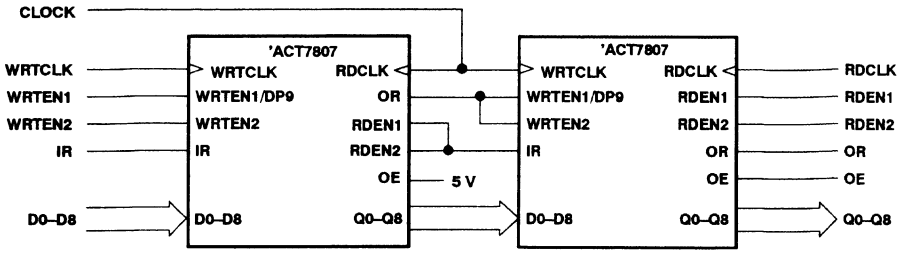



**Figure 5. Word-Depth Expansion: 4096 Words by 9 Bits**

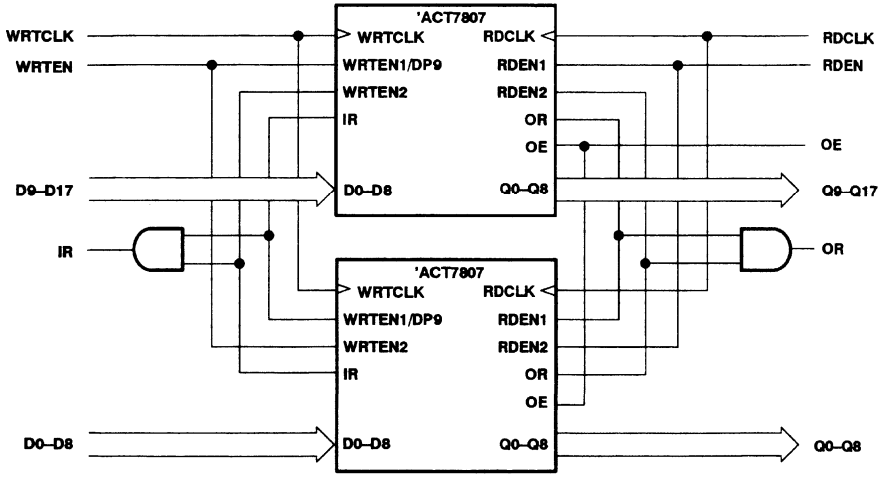



**Figure 6. Word-Width Expansion: 2048 Words by 18 Bits**

## TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

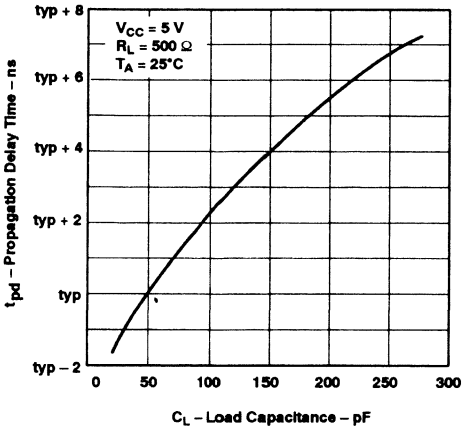



Figure 7

SUPPLY CURRENT
vs
CLOCK FREQUENCY

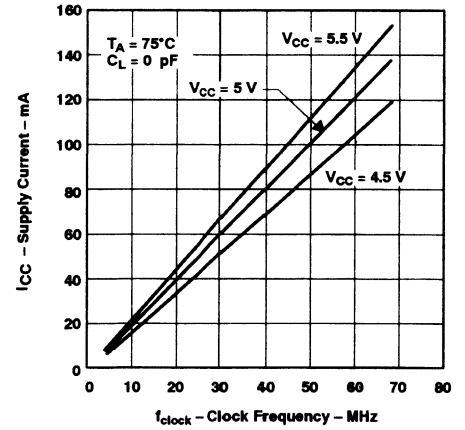



Figure 8

### calculating power dissipation

With $I_{CCF}$ taken from Figure 8, the maximum power dissipation may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

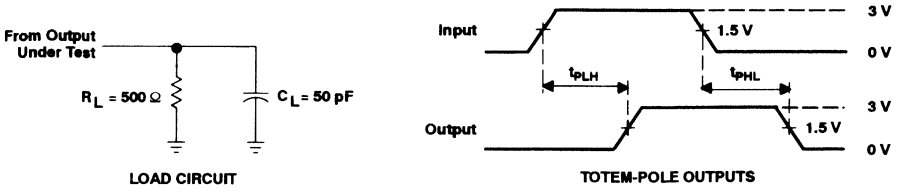
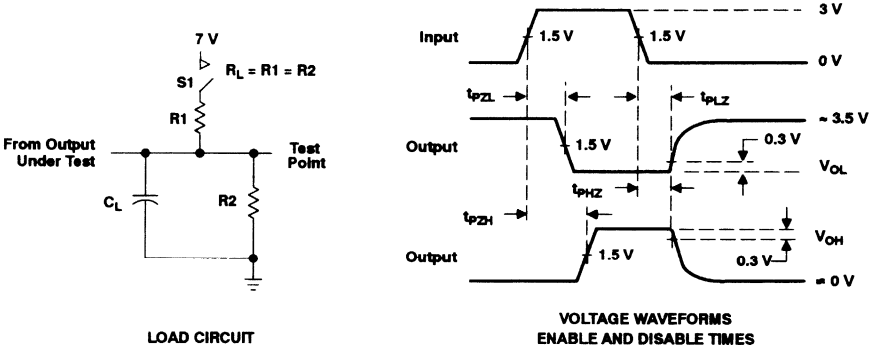



**Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)**



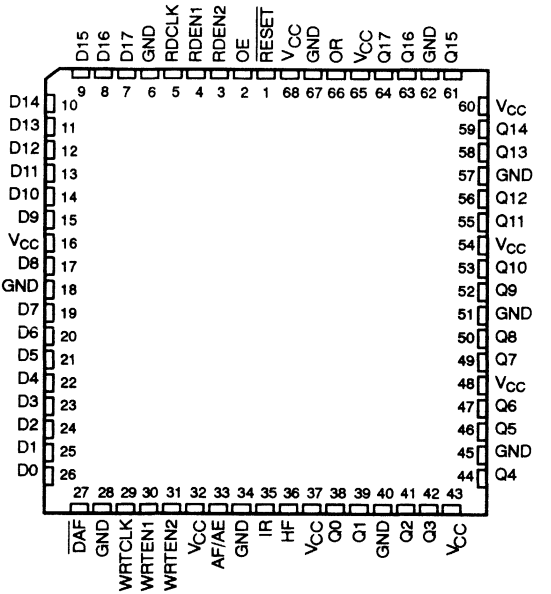

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

† Includes probe and test fixture capacitance.

**Figure 10. 3-State Outputs (Any Q)**

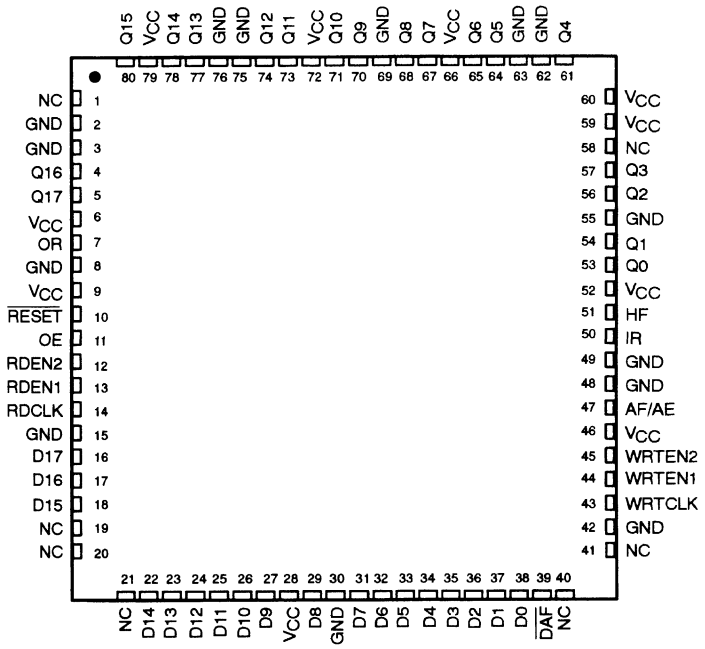
- Member of the Texas Instruments *Widebus*™ Family
- Independent Asynchronous Inputs and Outputs
- 1024 Words × 18 Bits
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost Full/Almost Empty Flag
- Input Ready, Output Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 15 ns With a 50-pF Load
- High Output Drive for Direct Bus Interface
- Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat Pack (PN)

FN PACKAGE
(TOP VIEW)




Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



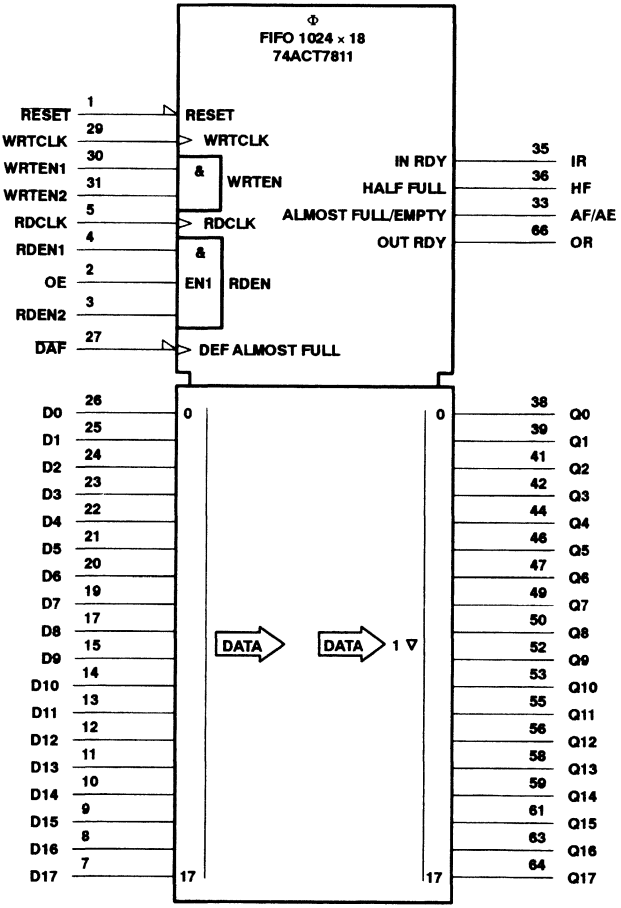

NC – No internal connection

## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7811 is a 1024- × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

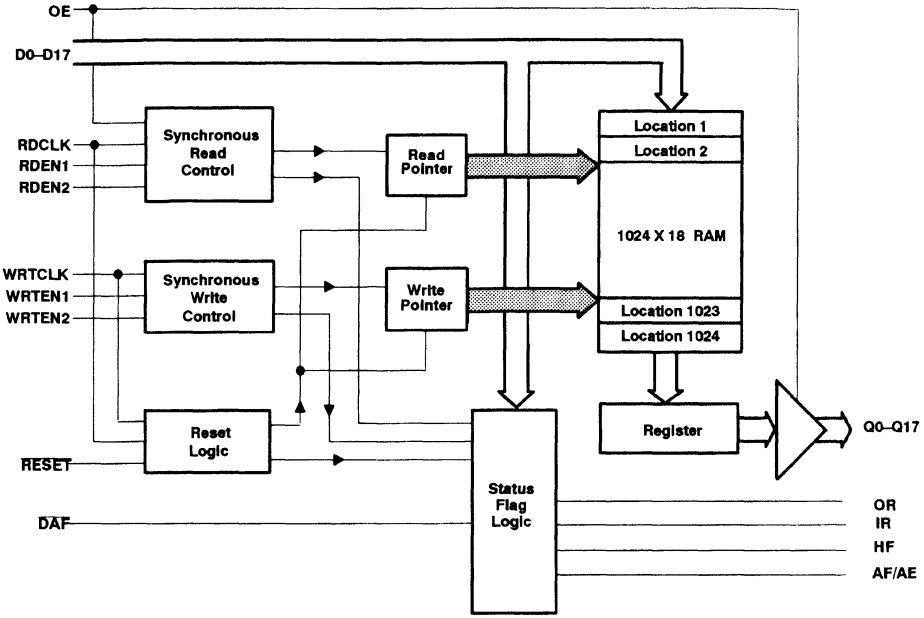
The SN74ACT7811 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts, requests) to their respective system clock.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for the FN package.

## functional block diagram




## terminal functions

### Inputs

**data in (D0–D17)**

Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0-D8 also carry the almost full/almost empty offset value (X) on a high-to-low transition of the define almost full ($\overline{DAF}$) input.

**reset ($\overline{RESET}$)**

A reset is accomplished by taking reset ($\overline{RESET}$) low and generating a minimum of four read clock (RDCLK) and write clock (WRTCLK) cycles. This ensures that the internal read and write pointers are reset and that the output ready flag (OR), the half-full flag (HF), and the input ready flag (IR) are low; the almost full/almost empty flag (AF/AE) is high. The FIFO must be reset upon power up. With the define almost full ($\overline{DAF}$) input at a low level, a low pulse on $\overline{RESET}$ defines the AF/AE status flag using the almost full/almost empty offset value (X), where X is the value previously stored. With $\overline{DAF}$ at a high level, a low-level pulse on $\overline{RESET}$ defines the AF/AE flag using the default value of X = 256.

**write enables (WRTEN1, WRTEN2)**

The write enables (WRTEN1, WRTEN2) must be high before the rising edge of write clock (WRTCLK) for a word to be written into memory. The write enables do not affect the storage of the almost full/almost empty offset value (X).

## terminal functions (continued)

**write clock (WRTCLK)**

Data is written into memory on a low-to-high transition of the write clock (WRTCLK) if the input ready flag output (IR) and the write enable control inputs (WRTEN1, WRTEN2) are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. The IR flag output is also driven synchronously with respect to the WRTCLK signal.

**read enables (RDEN1, RDEN2)**

Both read enables (RDEN1, RDEN2) must high before the rising edge of read clock (RDCLK) to read a word out of memory. The read enables are not used to read the first word stored in memory.

**read clock (RDCLK)**

Data is read out of memory on a low-to-high transition at the read clock (RDCLK) input if the output ready flag output (OR) and the output enable (OE) and read enable (RDEN1, RDEN2) control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. The OR flag is also driven synchronously with respect to the RDCLK signal.

**define almost full ($\overline{DAF}$)**

The high-to-low transition of the define almost full ($\overline{DAF}$) input stores the binary value of data inputs D0–D8 as the almost full/almost empty offset value (X). With $\overline{DAF}$ held low, a low pulse on the reset ($\overline{RESET}$) input defines the almost full/almost empty flag (AF/AE) using X.

**output enable (OE)**

The data out (Q0–Q17) outputs are in the high-impedance state when the output enable (OE) input is low. OE must be high before the rising edge of read clock (RDCLK) to read a word from memory.

**outputs**

**data out (Q0–Q17)**

The first data word to be loaded into the FIFO is moved to the data out (Q0–Q17) register on the rising edge of the third read clock (RDCLK) pulse to occur after the first valid write. The read enable (RDEN1, RDEN2) inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, and the output ready flag (OR) are high.

**Input ready flag (IR)**

The input ready flag (IR) is high when the FIFO is not full and low when the device is full. During reset, the IR flag is driven low on the rising edge of the second write clock (WRTCLK) pulse. The IR flag is driven high on the rising edge of the second WRTCLK pulse after $\overline{RESET}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.

**output ready flag (OR)**

The output ready flag (OR) is high when the FIFO is not empty and low when it is empty. During reset, the OR flag is set low on the rising edge of the third read clock (RDCLK) pulse. The OR flag is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.

**half-full status flag (HF)**

The half-full flag (HF) is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.

**almost full/almost empty status flag (AF/AE)**

The almost full/almost empty flag (AF/AE) is defined by the almost full/almost empty offset value (X). The AF/AE flag is high when the FIFO contains (X + 1) or less words or (1025 – X) or more words. The AF/AE flag is low when the FIFO contains between (X + 2) and (1024 – X) words.

**terminal functions (continued)**

**programming procedure for AF/AE**

The almost full/almost empty flag (AF/AE) is programmed during each reset cycle. The almost full/almost empty offset value (X) is either a user-defined value or the default value of X = 256. Below are instructions to program AF/AE using both methods .

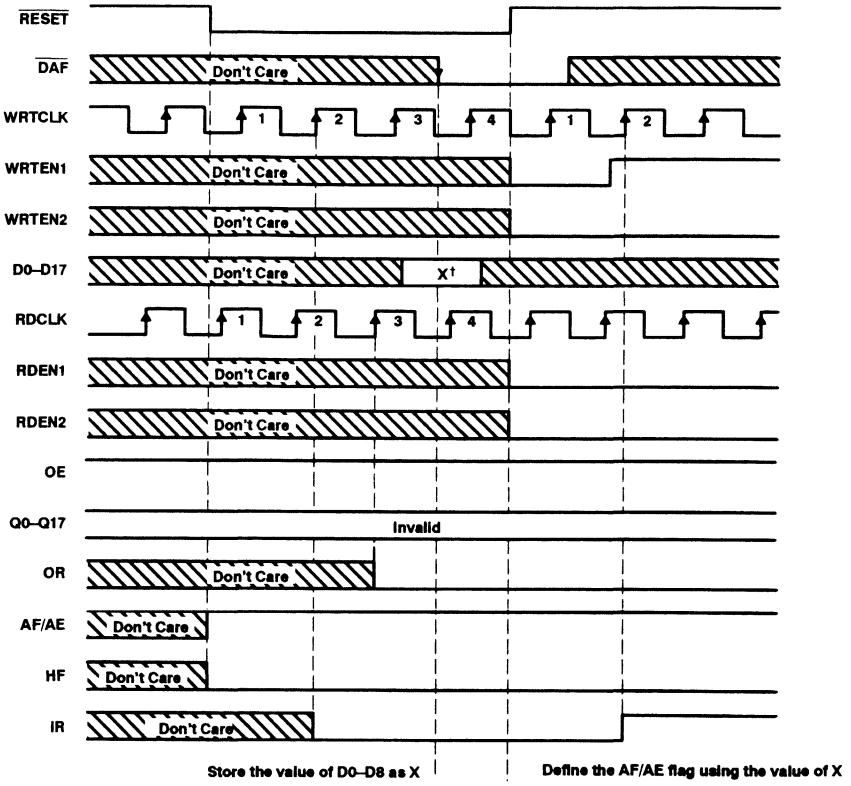
***user-defined X:***

Step 1. Take $\overline{DAF}$ from high to low.
Step 2. If $\overline{RESET}$ is not already low, take $\overline{RESET}$ low.
Step 3. With $\overline{DAF}$ held low, take $\overline{RESET}$ high. This defines the AF/AE flag using X.
Step 4. To retain the current offset for the next reset, keep $\overline{DAF}$ low.

***default X:***

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.

## timing diagrams




† X is the binary value of D0–D8 only.

**Figure 1. Reset Cycle: Define AF/AE Using the Value of X**

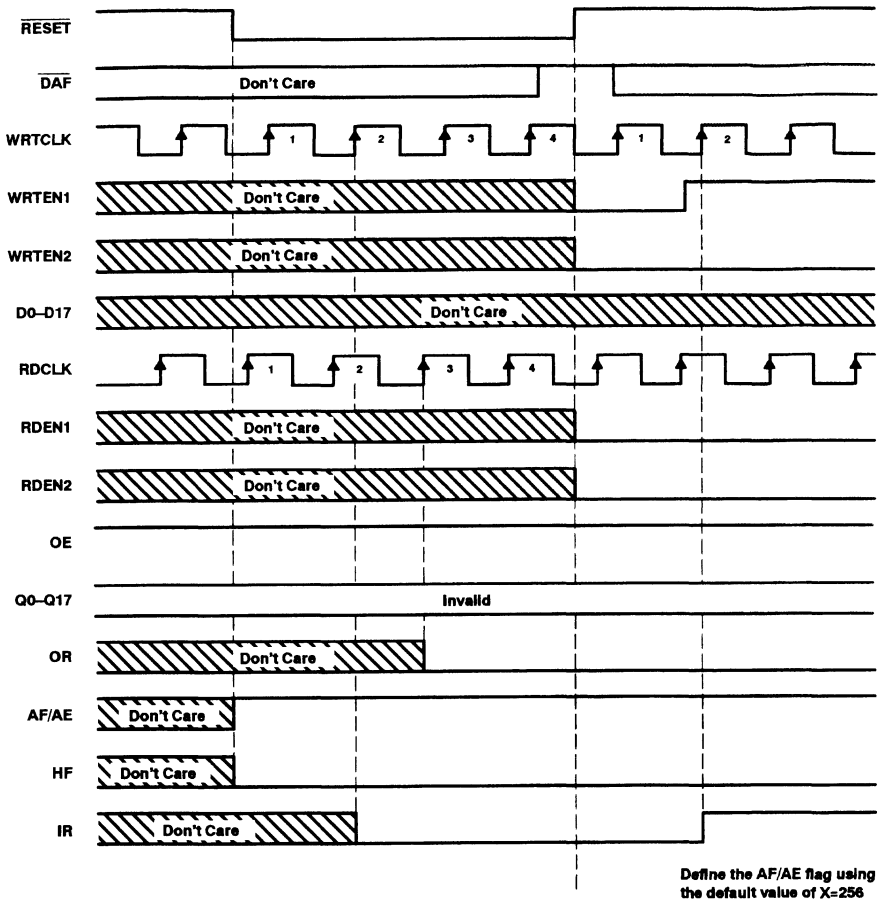



**Figure 2. Reset Cycle: Define AF/AE Using the Default Value**

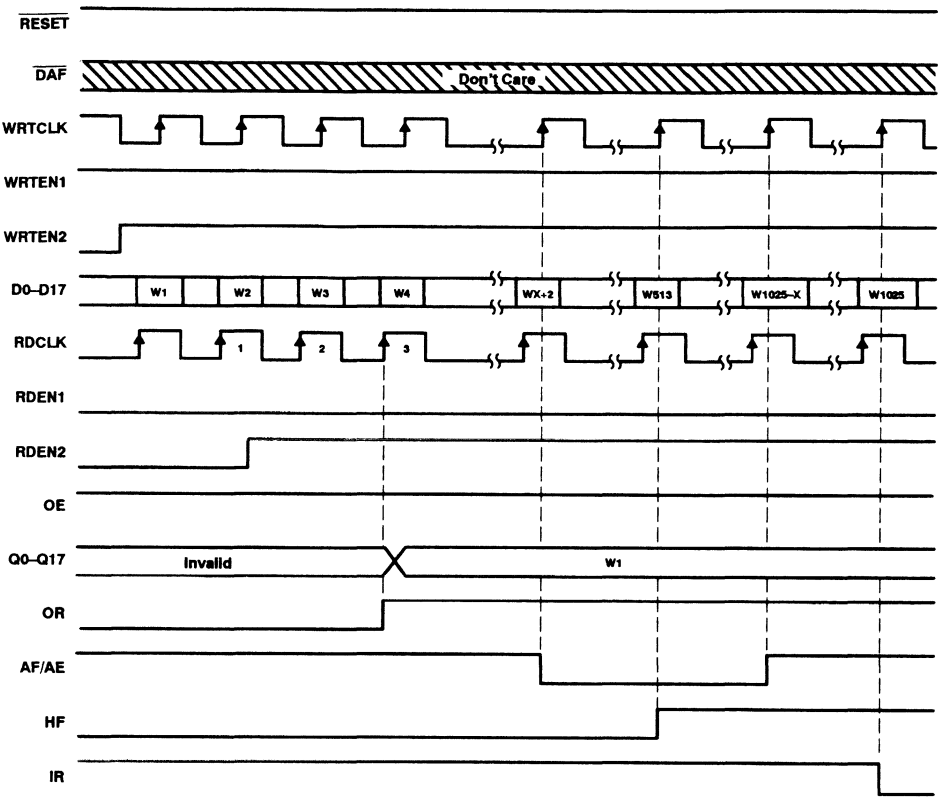



**Figure 3. Write**

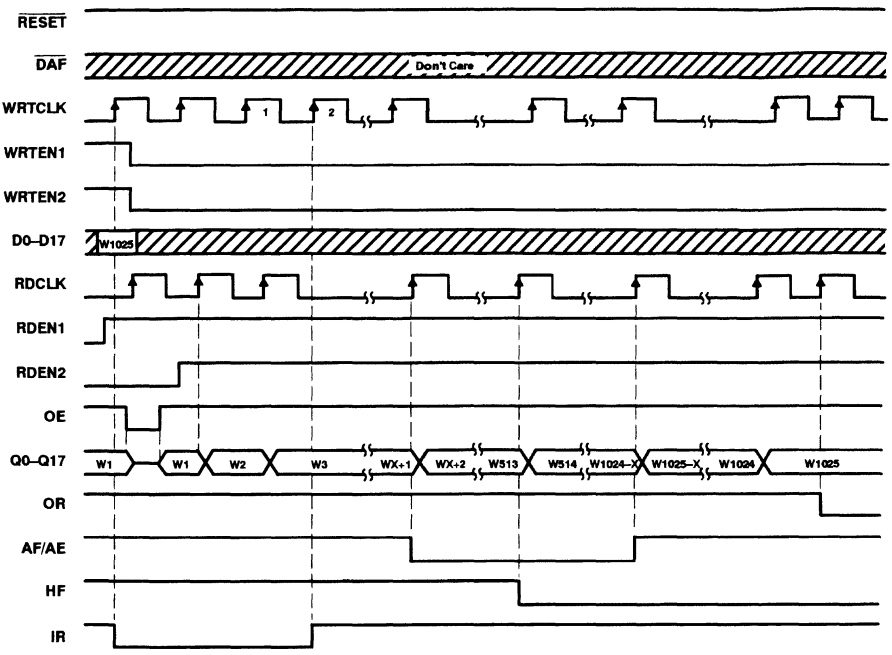



**Figure 4. Read**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −8 | mA |
| $I_{OL}$ | Low-level output current | | 16 | mA |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 4.5 V, | $I_{OH}$ = − 8 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | V |
| $I_I$ | Input current | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 V | | | ±5 | μA |
| $I_{OZ}$ | High-impedance-state output current | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 V | | | ±5 | μA |
| $I_{CC}$§ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 V | | | | 400 | μA |
| | | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0 V, f = 1 MHz | | | 4 | | pF |
| $C_o$ | | $V_O$ = 0 V, f = 1 MHz | | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ $I_{CC}$ tested with outputs open.

## timing requirements

| | | | 'ACT7811-15 | | 'ACT7811-18 | | 'ACT7811-20 | | 'ACT7811-25 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 40 | | 35 | | 28.5 | | 16.7 | | MHz |
| $t_w$ | Pulse duration | Data In (D0–D17) high or low | 10 | | 12 | | 14 | | 20 | | ns |
| | | WRTCLK high | 7 | | 8.5 | | 10 | | 17 | | |
| | | WRTCLK low | 10 | | 11 | | 14 | | 23 | | |
| | | RDCLK high | 7 | | 8.5 | | 10 | | 17 | | |
| | | RDCLK low | 10 | | 11 | | 14 | | 23 | | |
| | | $\overline{DAF}$ high | 10 | | 10 | | 10 | | 10 | | |
| | | WRTEN1, WRTEN2 high or low | 10 | | 10 | | 10 | | 10 | | |
| | | OE, RDEN1, RDEN2 high or low | 10 | | 10 | | 10 | | 10 | | |
| $t_{su}$ | Setup time | Data In (D0–D17) before WRTCLK↑ | 5 | | 5 | | 5 | | 5 | | ns |
| | | WRTEN1, WRTEN2 high before WRTCLK↑ | 5 | | 5 | | 5 | | 5 | | |
| | | OE, RDEN1, RDEN2 high before RDCLK↑ | 5 | | 5 | | 5 | | 5 | | |
| | | Reset: $\overline{RESET}$ low before first WRTCLK and RDCLK↑ | 7 | | 7 | | 7 | | 7 | | |
| | | Define AF/AE: D0–D8 before $\overline{DAF}$↓ | 5 | | 5 | | 5 | | 5 | | |
| | | Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑ | 7 | | 7 | | 7 | | 7 | | |
| | | Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑ | 5 | | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time | Data In (D0–D17) after WRTCLK↑ | 1 | | 1 | | 1 | | 1 | | ns |
| | | WRTEN1, WRTEN2 high after WRTCLK↑ | 1 | | 1 | | 1 | | 1 | | |
| | | OE, RDEN1, RDEN2 high after RDCLK↑ | 1 | | 1 | | 1 | | 1 | | |
| | | Reset: $\overline{RESET}$ low after fourth WRTCLK and RDCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE: D0–D8 after $\overline{DAF}$↓ | 1 | | 1 | | 1 | | 1 | | |
| | | Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑ | 1 | | 1 | | 1 | | 1 | | |

† To permit the clock pulse to be utilized for reset purposes.

## switching characteristics over recommended operating free-air temperature range (see Figures 9 and 10)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 0°C to 70°C† | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'ACT7811-15 | | | 'ACT7811-18 | | 'ACT7811-20 | | 'ACT7811-25 | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | WRTCLK or RDCLK | | 40 | | | 35 | | 28.5 | | 16.7 | | MHz |
| $t_{pd}$ | RDCLK↑ | Any Q | 4 | 12 | 15 | 4 | 18 | 4 | 20 | 4 | 25 | ns |
| $t_{pd}$‡ | | | | 10.5 | | | | | | | | |
| $t_{pd}$ | WRTCLK↑ | IR | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | ns |
| $t_{pd}$ | RDCLK↑ | OR | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | ns |
| $t_{pd}$ | WRTCLK↑ | AF/AE | 6 | | 20 | 6 | 22 | 6 | 24 | 6 | 26 | ns |
| $t_{pd}$ | RDCLK↑ | AF/AE | 6 | | 20 | 6 | 22 | 6 | 24 | 6 | 26 | ns |
| $t_{PLH}$ | WRTCLK↑ | HF | 6 | | 19 | 6 | 21 | 6 | 23 | 6 | 25 | ns |
| $t_{PHL}$ | RDCLK↑ | | 6 | | 19 | 6 | 21 | 6 | 23 | 6 | 25 | |
| $t_{PLH}$ | $\overline{RESET}$↓ | AF/AE | 3 | | 19 | 3 | 21 | 3 | 23 | 3 | 25 | ns |
| $t_{PHL}$ | | HF | 4 | | 21 | 4 | 23 | 4 | 25 | 4 | 27 | |
| $t_{en}$ | OE | Any Q | 2 | | 11 | 2 | 11 | 2 | 11 | 2 | 11 | ns |
| $t_{dis}$ | | | 2 | | 14 | 2 | 14 | 2 | 14 | 2 | 14 | |

† For conditions shown as MIN or MAX, use the appropriate value under recommended operating conditions.
‡ This parameter is measured with $C_L$ = 30 pF (see Figure 5).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per 1K bits | $C_L$ = 50 pF, f = 5 MHz | 65 | pF |

## TYPICAL CHARACTERISTICS

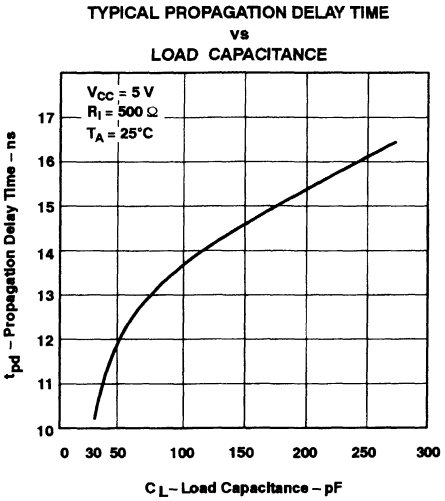
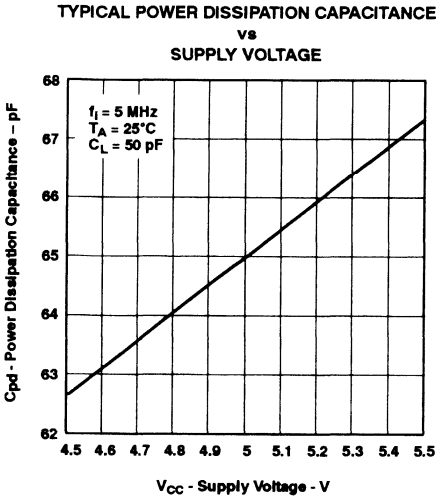



Figure 5

## TYPICAL CHARACTERISTICS




$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

**Figure 6**

## APPLICATION DATA

### expanding the SN74ACT7811

The SN74ACT7811 is expandable in width and depth. Expanding in word depth offers special timing considerations:

1. After the first data word is loaded into the FIFO, the word is unloaded, and the output ready flag output (OR) goes high after (N × 3) read clock (RDCLK) cycles, where N is the number of devices used in depth expansion.
2. After the FIFO is filled, the input ready flag output (IR) goes low, the first word is unloaded, and the IR flag output is driven high after (N × 2) write clock cycles, where N is the number of devices used in depth expansion.

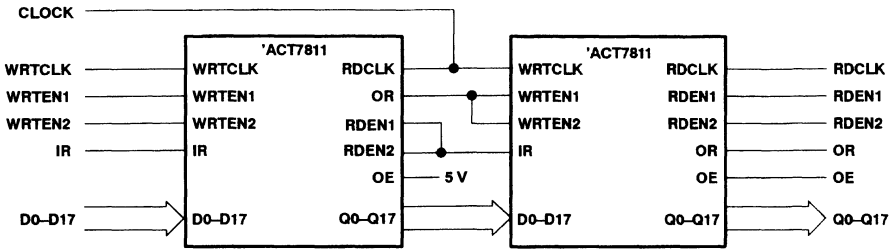



**Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2**

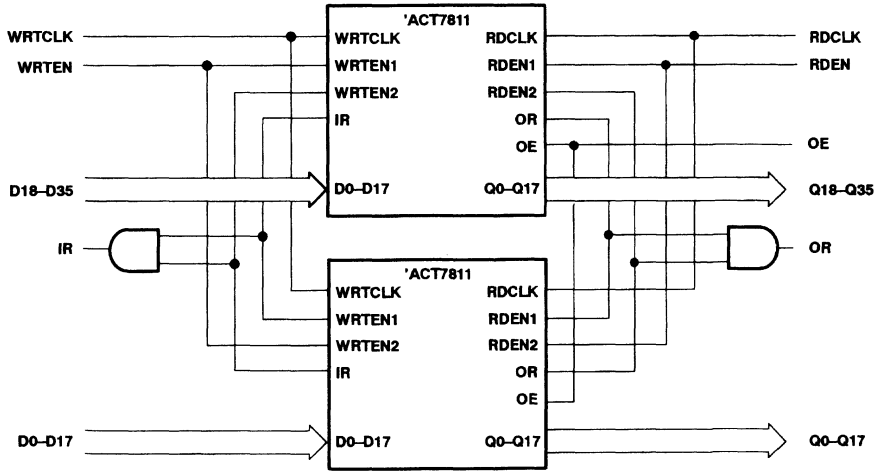



**Figure 8. Word-Width Expansion: 1024 Words × 36 Bits**

## PARAMETER MEASUREMENT INFORMATION

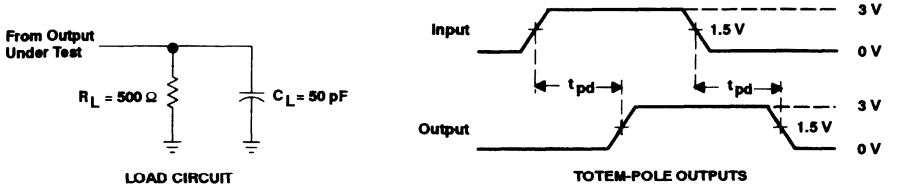
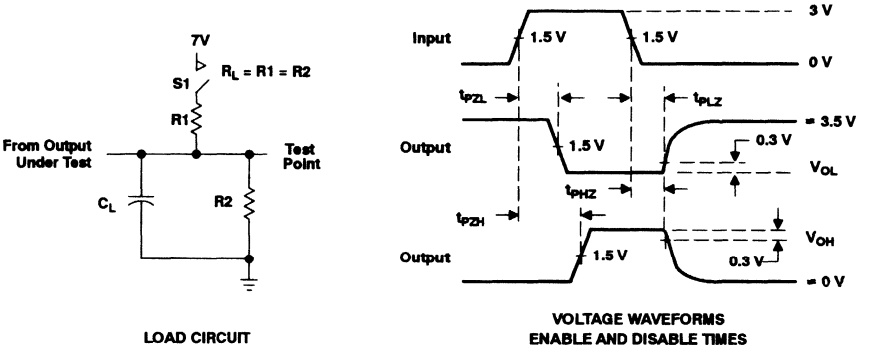



**Figure 9. Standard CMOS Outputs**



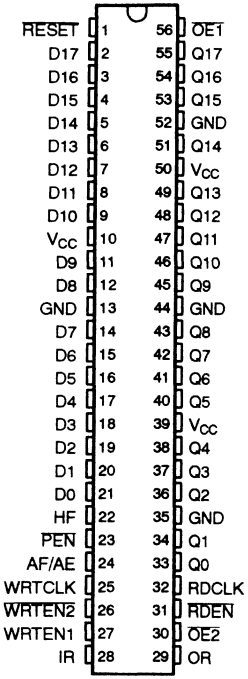

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

† Includes probe and test fixture capacitance.

**Figure 10. 3-State Outputs (Any Q)**

- **Member of the Texas Instruments *Widebus*™ Family**
- **Free-Running Read and Write Clocks May Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**
- **64 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost Full/Almost Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7803 and SN74ACT7805**

DL PACKAGE
(TOP VIEW)




## description

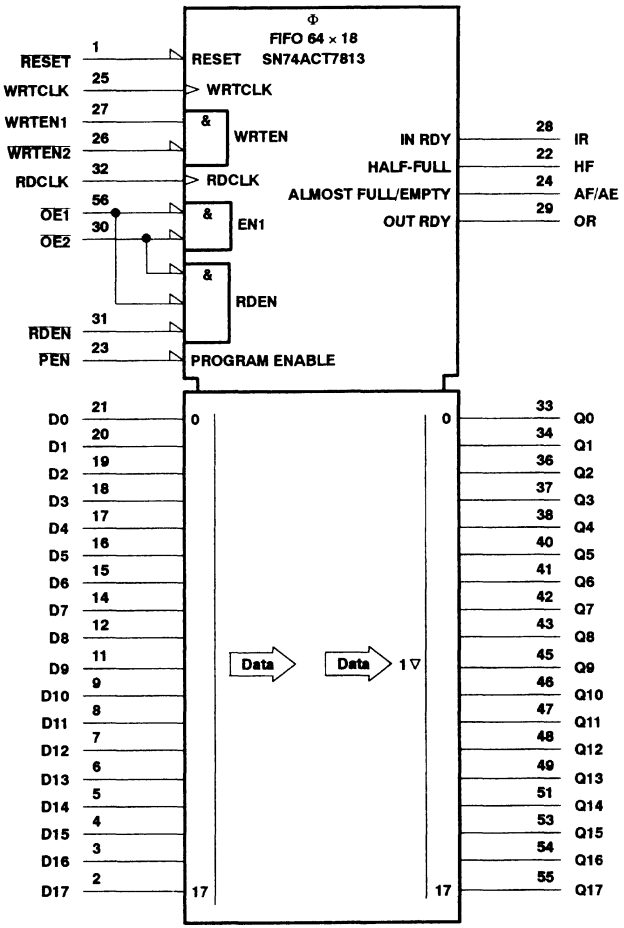
The SN74ACT7813 is a 64-word × 18-bit FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices may be configured for bidirectional data buffering without additional logic. Multiple distributed $V_{CC}$ and GND pins along with TI's patented Output Edge Control (OEC™) circuit dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) should be free-running and may be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO may be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

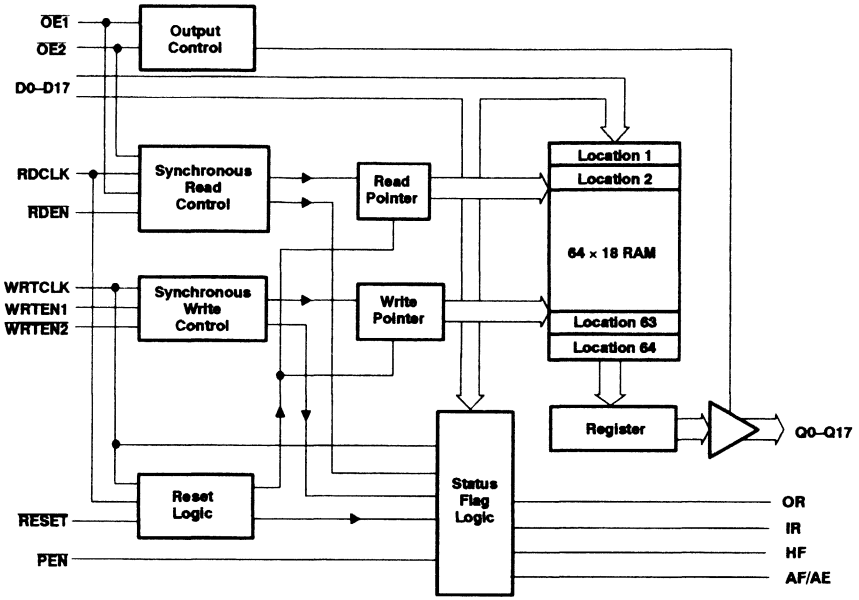
Widebus and OEC are trademarks of Texas Instruments Incorporated.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

## functional block diagram



## Terminal Functions

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AF/AE | 24 | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 8 may be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (64 minus Y) or more words. AF/AE is high after reset. |
| D0–D17 | 21–14, 12–11, 9–2 | I | 18-bit data input port |
| HF | 22 | O | Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset. |
| IR | 28 | O | Input ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset. |
| $\overline{OE1}$, $\overline{OE2}$ | 56, 30 | I | Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled, and the data outputs are in the high-impedance state. |
| OR | 29 | O | Output ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory. |
| $\overline{PEN}$ | 23 | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high. |
| Q0–Q17 | 33–34, 36–38, 40–43, 45–49, 51, 53–55 | O | 18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17. |
| RDCLK | 32 | I | Read clock. RDCLK is a continuous clock and may be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK. |
| $\overline{RDEN}$ | 31 | I | Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK. |
| $\overline{RESET}$ | 1 | I | Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high. |
| WRTCLK | 25 | I | Write clock. WRTCLK is a continuous clock and may be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK. |
| WRTEN1, $\overline{WRTEN2}$ | 27, 26 | I | Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK. |

## timing diagram

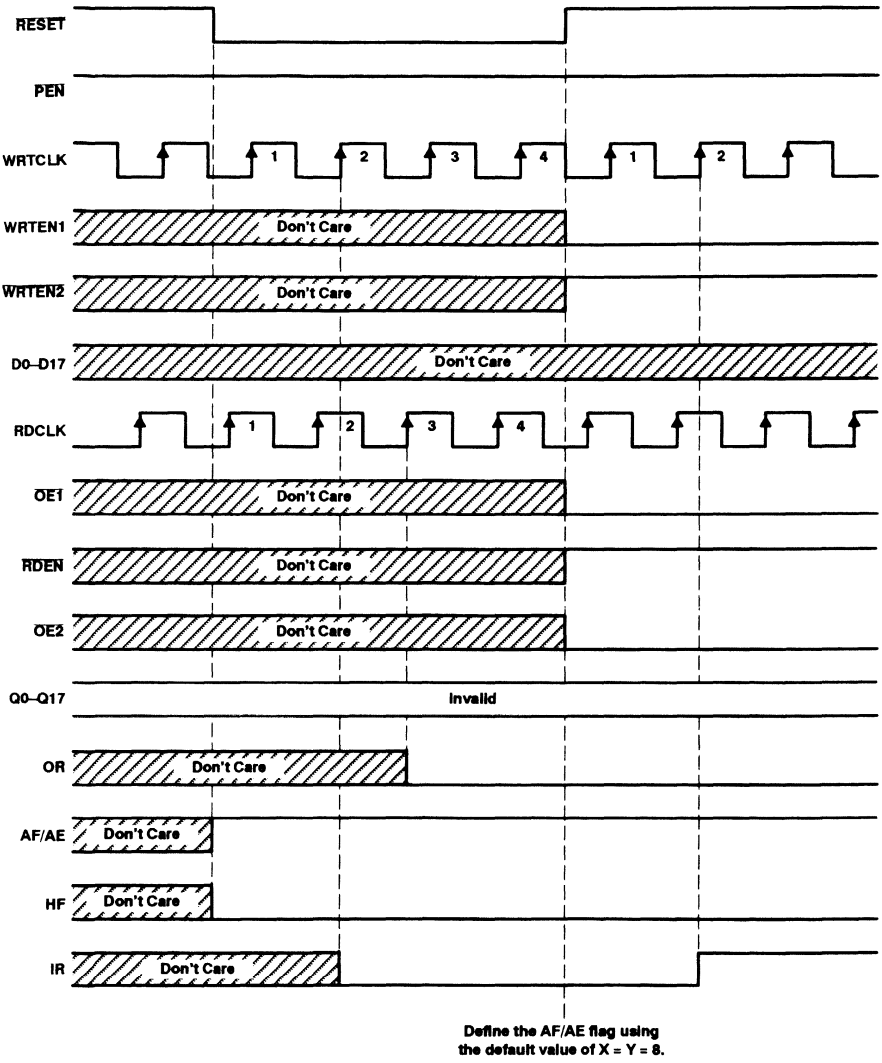



Figure 1. Reset Cycle

## timing diagram

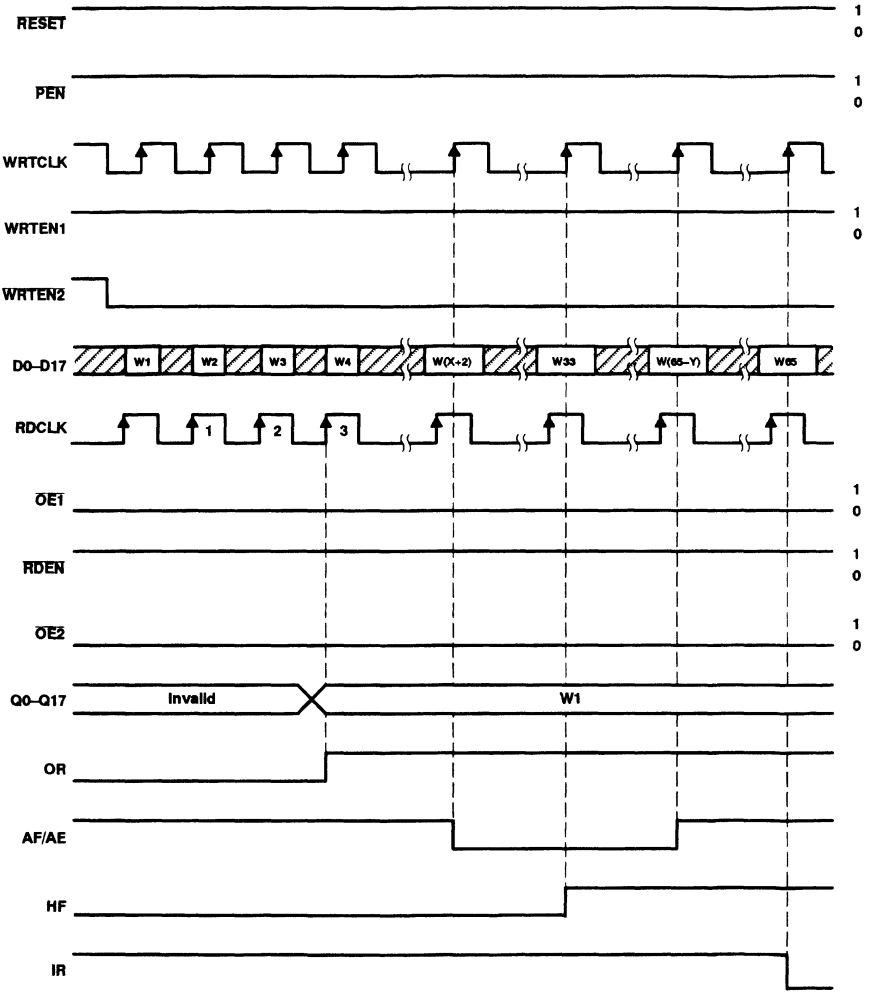



Figure 2. Write

## timing diagram

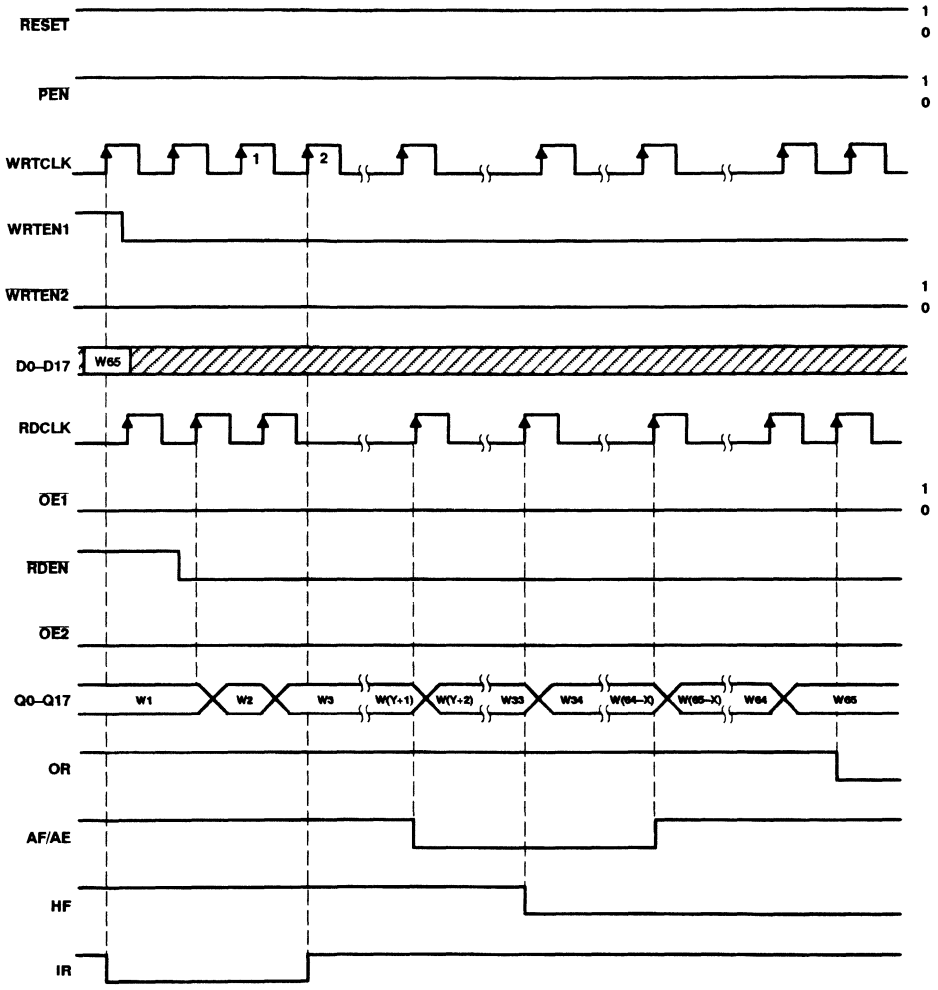



**Figure 3. Read**

### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost empty offset value (X) and the almost full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 8 are used. The AF/AE flag is high when the FIFO contains X or less words or (64 minus Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ may be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0-D4 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK will reprogram Y to the binary value on D0–D4 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{WRTEN2}$). A maximum value of 31 may be programmed for either X or Y. To use the default values of X = Y = 8, $\overline{PEN}$ must be held high.

### timing diagram

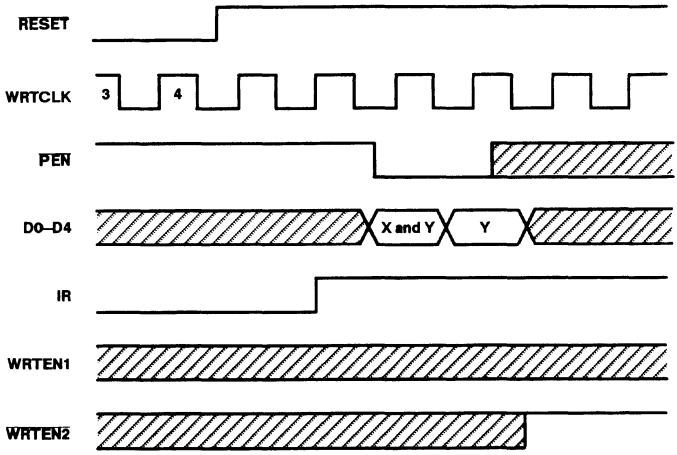



**Figure 4. Programming X and Y Separately**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage, $V_I$ | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | 'ACT7813-15 | | 'ACT7813-20 | | 'ACT7813-25 | | 'ACT7813-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 67 | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | WRTCLK high or low | 6 | | 7 | | 8 | | 12 | | ns |
| | | RDCLK high or low | 6 | | 7 | | 8 | | 12 | | |
| | | $\overline{PEN}$ low | 8 | | 9 | | 9 | | 12 | | |
| $t_{su}$ | Setup time | Data in (D0–D17) before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | ns |
| | | $\overline{WRTEN1}$, $\overline{WRTEN2}$ before WRTCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| | | $\overline{OE1}$, $\overline{OE2}$ before RDCLK↑ | 5 | | 5 | | 6 | | 6 | | |
| | | $\overline{RDEN}$ before RDCLK↑ | 4 | | 5 | | 5 | | 5 | | |
| | | Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑† | 5 | | 6 | | 6 | | 6 | | |
| | | $\overline{PEN}$ before WRTCLK↑ | 5 | | 6 | | 6 | | 6 | | |
| $t_h$ | Hold time | Data in (D0–D17) after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | ns |
| | | $\overline{WRTEN1}$, $\overline{WRTEN2}$ after WRTCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | $\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑† | 2 | | 2 | | 2 | | 2 | | |
| | | $\overline{PEN}$ high after WRTCLK↓ | 0 | | 0 | | 0 | | 0 | | |
| | | $\overline{PEN}$ low after WRTCLK↑ | 2 | | 2 | | 2 | | 2 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

† To permit the clock pulse to be utilized for reset purposes.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$‡ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 9 and 10)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7813-15 | | | 'ACT7813-20 | | 'ACT7813-25 | | 'ACT7813-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | WRTCLK or RDCLK | | 67 | | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | RDCLK↑ | Any Q | 4 | 9.5 | 12 | 4 | 13 | 4 | 15 | 4 | 20 | ns |
| $t_{pd}$§ | | | | 8.5 | | | | | | | | |
| $t_{pd}$ | WRTCLK↑ | IR | 3 | | 8.5 | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | RDCLK↑ | OR | 3 | | 8.5 | 3 | 11 | 3 | 13 | 3 | 15 | ns |
| $t_{pd}$ | WRTCLK↑ | AF/AE | 7 | | 16.5 | 7 | 19 | 7 | 21 | 7 | 23 | ns |
| $t_{pd}$ | RDCLK↑ | AF/AE | 7 | | 17 | 7 | 19 | 7 | 21 | 7 | 23 | ns |
| $t_{PLH}$ | WRTCLK↑ | HF | 7 | | 15 | 7 | 17 | 7 | 19 | 7 | 21 | ns |
| $t_{PHL}$ | RDCLK↑ | | 7 | | 15.5 | 7 | 18 | 7 | 20 | 7 | 22 | |
| $t_{PLH}$ | $\overline{RESET}$ low | AF/AE | 2 | | 9 | 2 | 11 | 2 | 13 | 2 | 15 | ns |
| $t_{PHL}$ | | HF | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | |
| $t_{en}$ | $\overline{OE1}$, $\overline{OE2}$ | Any Q | 2 | | 8.5 | 2 | 11 | 2 | 11 | 2 | 11 | ns |
| $t_{dis}$ | | | 2 | | 9.5 | 2 | 11 | 2 | 14 | 2 | 14 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

§ This parameter is measured with a 30 pF load (see Figure 7).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | 53 | pF |

## APPLICATION DATA

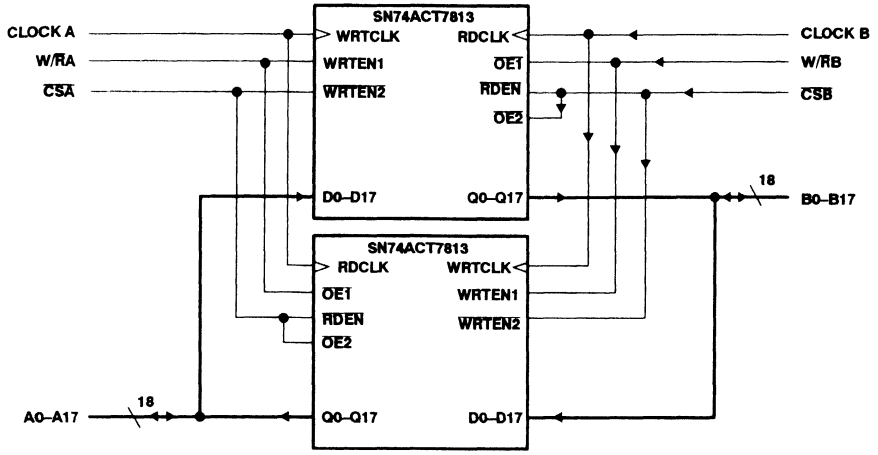



**Figure 5. Bidirectional Configuration**

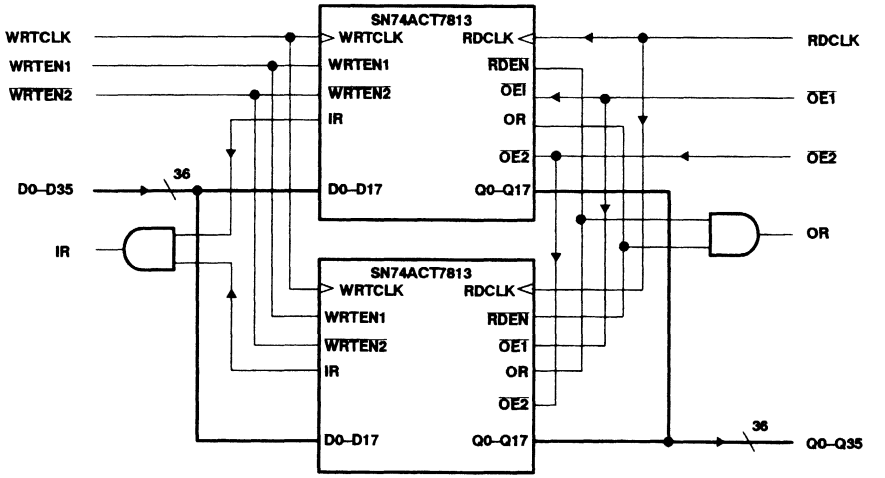



**Figure 6. Word-Width Expansion: 64 × 36 Bits**

## TYPICAL CHARACTERISTICS

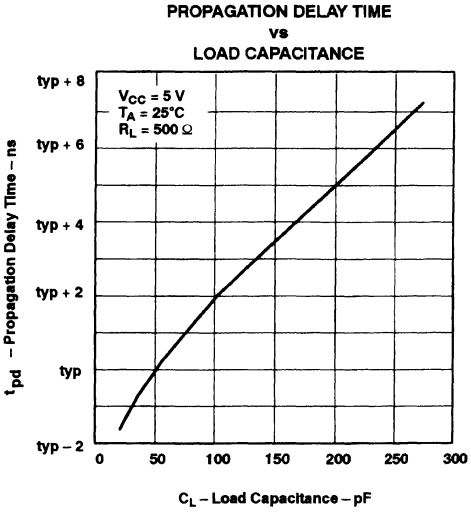



Figure 7

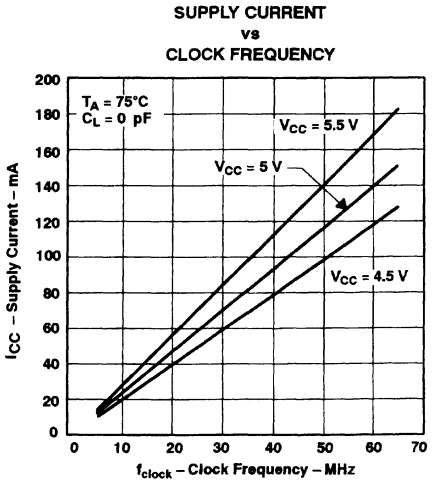



Figure 8

### calculating power dissipation

With $I_{CCF}$ taken from Figure 8, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_{pd} \times V_{CC}^2 \times fi) + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta\ I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

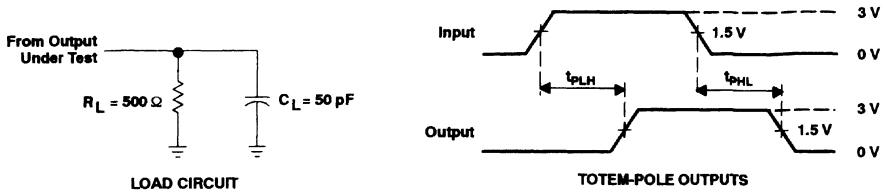
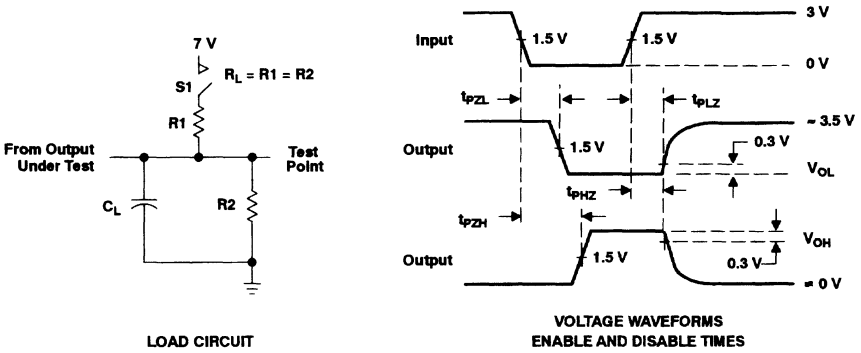



**Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)**



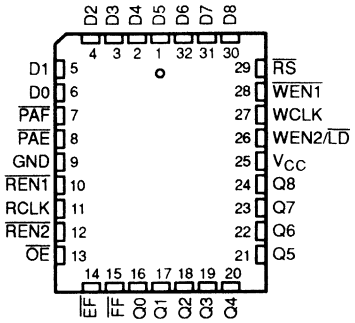

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

† Includes probe and test fixture capacitance.

**Figure 10. 3-State Outputs (Any Q)**

- **Read and Write Clocks May Be Asynchronous or Coincident**
- **Organization:**
  - **SN74ACT72211L – 512 × 9**
  - **SN74ACT72221L – 1024 × 9**
  - **SN74ACT72231L – 2048 × 9**
  - **SN74ACT72241L – 4096 × 9**
- **Write and Read Cycle Times of 15 ns**
- **Bit-Width Expandable**
- **Empty and Full Flags**
- **Programmable Almost-Empty and Almost-Full Flags With Default Offsets of Empty+7 and Full–7, Respectively**
- **Available in 32-Pin Plastic Leaded Chip Carrier (PLCC)**
- **TTL-Compatible Inputs**
- **Fully Compatible With the IDT72211/72221/72231/72241**

**RJ PACKAGE**
**(TOP VIEW)**




## description

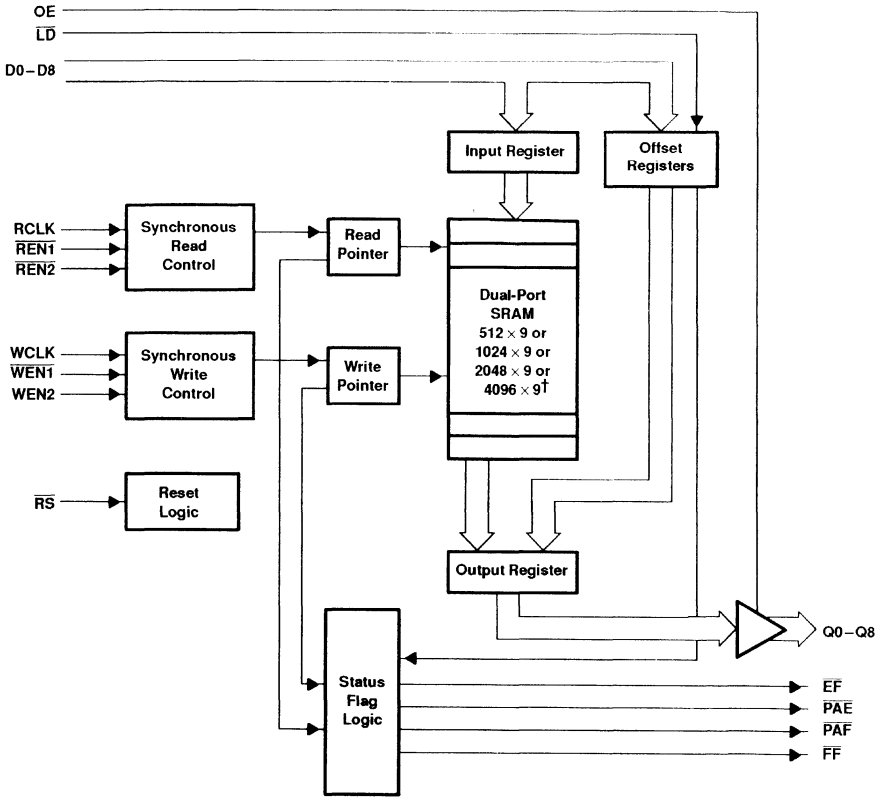
The SN74ACT72211L, SN74ACT72221L, SN74ACT72231L, and SN74ACT72241L are constructed with CMOS dual-port SRAM and are arranged as 512, 1024, 2048, and 4096 9-bit words, respectively. Internal write and read address counters provide data throughput on a first-in, first-out (FIFO) basis. The SN74ACT72211L, –72221L, -72231L, and -72241L support write and read clock frequencies up to 66.7 MHz. Full and empty flags prevent memory overflow and underflow, and two programmable flags (almost full and almost empty) are provided.

The SN74ACT72211L, SN74ACT72221L, SN74ACT72231L, and SN74ACT72241L are clocked FIFOs, which means the data input port and data output port each employ synchronous control. Write-enable ($\overline{WEN1}$, WEN2/$\overline{LD}$) signals allow the low-to-high transition of the write clock (WCLK) to store data in memory, and read-enable ($\overline{REN1}$, $\overline{REN2}$) signals allow the low-to-high transition of the read clock (RCLK) to read data from memory. WCLK and RCLK are independent of one another and may operate asynchronously or be tied together for single-clock operation.

The empty flag ($\overline{EF}$) output is synchronized to RCLK and the full flag ($\overline{FF}$) output is synchronized to WCLK to indicate absolute boundary conditions. Write operations are prohibited when $\overline{FF}$ is low, and read operations are prohibited when $\overline{EF}$ is low. Two programmable flags, programmable almost empty ($\overline{PAE}$) and programmable almost full ($\overline{PAF}$), can both be programmed to indicate any measure of memory fill. After reset, $\overline{PAE}$ defaults to empty+7 and $\overline{PAF}$ defaults to full–7. Flag offset programming control is similar to a memory write with the use of the load (WEN2/$\overline{LD}$) signal.

These devices are suited for providing a data channel between two buses operating at asynchronous or synchronous rates. Applications include use as rate buffers for graphics systems and high-speed queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information.

## functional block diagram




† 512 × 9 for the SN74ACT72211L; 1024 × 9 for the SN74ACT72221L; 2048 × 9 for the SN74ACT72231L; 4096 × 9 for the SN74ACT72241L

## Terminal Functions

| PIN NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| D0 – D8 | 6 – 1, 32 – 30 | I | Data inputs |
| $\overline{EF}$ | 14 | O | Empty-flag output. When memory is empty, the empty-flag output is low, and further data reads are ignored by the device. When $\overline{EF}$ is high, the memory is not empty, and data reads are allowed. $\overline{EF}$ is synchronized to the read clock (RCLK) by one flip-flop. |
| $\overline{FF}$ | 15 | O | Full-flag output. When memory is full, the full-flag output is low, and data writes are inhibited. $\overline{FF}$ is synchronized to the write clock (WCLK) by one flip-flop. |
| GND | 9 | | Ground |
| $\overline{OE}$ | 13 | I | Output-enable input. The data (Q0 – Q8) outputs are in the high-impedance state when $\overline{OE}$ is high. The Q0 – Q8 outputs are active when $\overline{OE}$ is low. |
| $\overline{PAE}$ | 8 | O | Programmable almost-empty-flag output. $\overline{PAE}$ is low when the FIFO is almost empty based on the value in its offset register. The default value for the register is empty+7. $\overline{PAE}$ is synchronized to the read clock (RCLK) by one flip-flop. |
| $\overline{PAF}$ | 7 | O | Programmable almost-full-flag output. $\overline{PAF}$ is low when the FIFO is almost full based on the value in its offset register. The default value for the register is full – 7. $\overline{PAF}$ is synchronized to the write clock (WCLK) by one flip-flop. |
| Q0 – Q8 | | O | Data outputs |
| RCLK | 11 | I | Read-clock input. A data read is performed by the low-to-high transition of RCLK when the read enables ($\overline{REN1}$, $\overline{REN2}$) are asserted and the empty flag ($\overline{EF}$) is high. |
| $\overline{REN1}$, $\overline{REN2}$ | 10, 11 | I | Read-enable inputs. Data is read from the FIFO on a low-to-high transition of read clock (RCLK) when $\overline{REN1}$ and $\overline{REN2}$ are low and the empty flag ($\overline{EF}$) is high. |
| $\overline{RS}$ | 29 | I | Reset input. When $\overline{RS}$ is set low, the read and write pointers are initialized to the first RAM location, and the FIFO is empty. The full flag ($\overline{FF}$) and programmable almost-full flag ($\overline{PAF}$) are set high, and the empty flag ($\overline{EF}$) and programmable almost-empty flag ($\overline{PAE}$) are set low. Each bit in the data output register is set low by a device reset. The FIFO must be reset after power up before data is written. |
| $V_{CC}$ | | | Supply voltage |
| WCLK | 27 | I | Write-clock input. Data is written by the low-to-high transition of WCLK when the write enables are asserted and the full flag ($\overline{FF}$) is high. |
| $\overline{WEN1}$ | 28 | I | Write-enable 1 input. If the device is configured to have programmable flags, $\overline{WEN1}$ is the only write enable pin, and data is written on a low-to-high transition of write clock (WCLK) when $\overline{WEN1}$ is low and the full flag ($\overline{FF}$) is high. If the FIFO is not configured for programmable flags, data is written on a low-to-high transition of WCLK when $\overline{WEN1}$ and write enable 2 (WEN2) are asserted and $\overline{FF}$ is high. |
| WEN2/$\overline{LD}$ | 26 | I | Write-enable 2/load input. This is a dual-purpose input. The FIFO may have either two write enables or programmable flags. To use WEN2/$\overline{LD}$ as a write enable (WEN2), WEN2/$\overline{LD}$ must be held high at reset. Then, when WEN2 and write enable 1 ($\overline{WEN1}$) are asserted and the full flag ($\overline{FF}$) is high, a low-to-high transition of write clock (WCLK) writes data. To use WEN2/$\overline{LD}$ as the load ($\overline{LD}$) pin, it must be held low at reset. In this case, $\overline{LD}$ is asserted low to write or read the programmable offset registers. |

## detailed description

### device reset

A reset is performed by taking the reset ($\overline{RS}$) input low. This initializes both the write and read pointers to the first memory location. After a reset, the full flag ($\overline{FF}$) and programmable almost-full flag ($\overline{PAF}$) are high, and the empty flag ($\overline{EF}$) and programmable almost-empty flag ($\overline{PAE}$) are low. Each bit in the data output register (Q0–Q8) is set low, and the flag offset registers are loaded with the default offset values. A FIFO must be reset after power up before a write cycle is allowed.

The logic level on the dual-purpose input write enable 2/load (WEN2/$\overline{LD}$) during reset determines its function. If WEN2/$\overline{LD}$ is high when $\overline{RS}$ returns high at the end of the reset cycle, the pin operates only as a second write enable (see *FIFO writes and reads* below), and the programmable flags ($\overline{PAF}$, $\overline{PAE}$) may only use the default values. If WEN2/$\overline{LD}$ is low when $\overline{RS}$ returns high at the end of the reset cycle, the pin operates only as the load ($\overline{LD}$) enable for writing and reading flag offset registers (see *flag programming* below).

### FIFO writes and reads

Data is written to memory by a low-to-high transition of write clock (WCLK) when write enable 1 ($\overline{WEN1}$) is low, WEN2/$\overline{LD}$ is high, and $\overline{FF}$ is high. This stores D0–D8 data in the dual-port SRAM and increments the write pointer.

If no reads are performed after reset ($\overline{RS}$ = $V_{IL}$), $\overline{FF}$ is set low upon the completion of 512 writes to the SN74ACT72211, 1024 writes to the SN74ACT72221, 2048 writes to the SN74ACT72231, and 4096 writes to the SN74ACT72241. Attempted write cycles are ignored when $\overline{FF}$ is low. $\overline{FF}$ is set high by the first low-to-high transition of WCLK after data is read from a full FIFO. $\overline{FF}$ and $\overline{PAF}$ are each synchronized to the low-to-high transition of WCLK by one flip-flop.

If a device is configured to have two write enables (see *device reset* above), data is read by the low-to-high transition of read clock (RCLK) when both read enables ($\overline{REN1}$, $\overline{REN2}$) are low and $\overline{EF}$ is high. WEN2/$\overline{LD}$ must also be high if the device is configured to have programmable flags. A read from the FIFO puts RAM data on Q0–Q8 and increments the read pointer in the same sequence as the write pointer. New data is not shifted to the output register while either one or both of the read enables are high.

$\overline{EF}$ and $\overline{PAE}$ are each synchronized to the low-to-high transition of RCLK by one flip-flop. When the device is empty, the write and read pointers are equal, and $\overline{EF}$ is set low. Attempted read cycles are ignored while $\overline{EF}$ is set low. $\overline{EF}$ is set high by the first low-to-high transition of RCLK after data is written to an empty FIFO.

WCLK and RCLK may be asynchronous or coincident to one another. Writing data to FIFO memory is independent of reading data from FIFO memory and vice versa.

### flag programming

When WEN2/$\overline{LD}$ is held low during a device reset ($\overline{RS}$ = $V_{IL}$), the pin acts only as the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 8-bit offset registers contained in the SN74ACT72211L/-72221L/-72231L/-72241L for writing or reading data.

When the device is configured for programmable flags and both WEN2/$\overline{LD}$ and $\overline{WEN1}$ are low, the first low-to-high transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth low-to-high transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{LD}$ and $\overline{WEN1}$ are low. The fifth low-to-high transition of WCLK while WEN2/$\overline{LD}$ and $\overline{WEN1}$ are low writes data to the empty LSB register again. Figure 1 shows the register sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers may be written; then, by bringing the WEN2/$\overline{LD}$ input high, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{LD}$ is brought low, a write operation will store data in the next offset register in sequence.

**flag programming (continued)**

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{LD}$ is low and both $\overline{REN1}$ and $\overline{REN2}$ are low. Low-to-high transitions of RCLK read the register contens to the data outputs. Writes and reads should not be performed simultaneously on the offset registers.

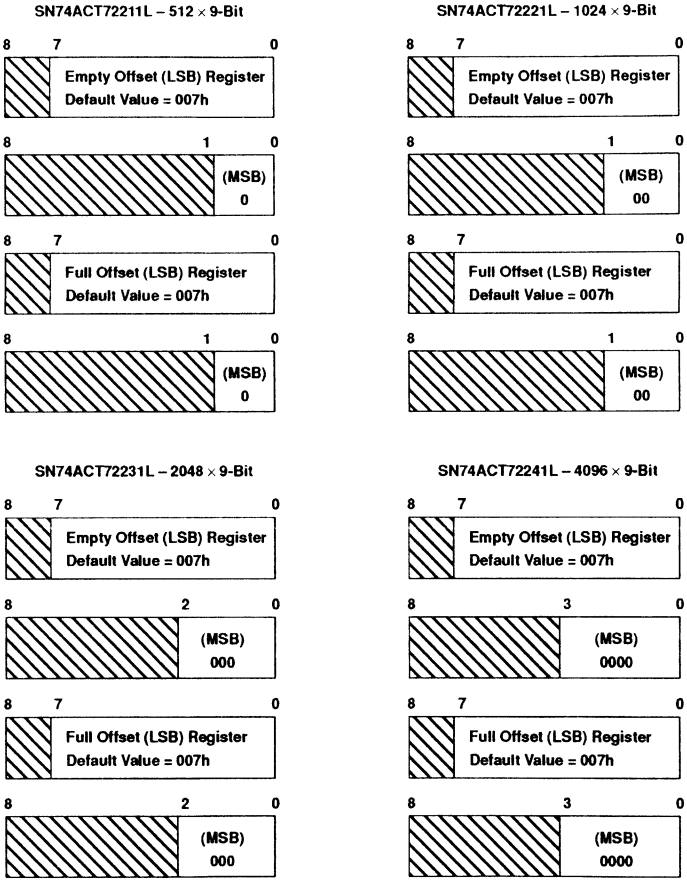



**Figure 1. Offset Register Location and Default Values**

## detailed description (continued)

DXXXXWRITING THE OFFSET REGISTERS

| $\overline{LD}$ | $\overline{WEN1}$ | WCLK† | SELECTION |
|---|---|---|---|
| 0 | 0 | ↑ | Empty offset (LSB)<br>Empty offset (MSB)<br>Full offset (LSB)<br>Full offset (MSB) |
| 0 | 1 | ↑ | No operation |
| 1 | 0 | ↑ | Write into FIFO |
| 1 | 1 | ↑ | No operation |

† The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the low-to-high transition of RCLK.

### programmable flag ($\overline{PAE}$, $\overline{PAF}$) operation

Whether the flag offset registers are programmed as described above or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the low-to-high transition of RCLK by one flip-flop and is low when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set high by the low-to-high transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAF}$ is synchronized to the low-to-high transition of WCLK by one flip-flop and is set low when the number of unread words in the FIFO is greater then or equal to (512-m) for the SN74ACT72211L, (1024-m) for the SN74ACT72221L, (2048-m) for the SN74ACT72231L, and (4096-m) for the SN74ACT72241L. $\overline{PAF}$ is set high by the low-to-high transition of WCLK when the number of available memory locations is greater than m.

STATUS FLAG TABLE

| NUMBER OF WORDS IN FIFO | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| SN74ACT72211L | SN74ACT72221L | SN74ACT72231L | SN74ACT72241L | $\overline{FF}$ | $\overline{PAF}$ | $\overline{PAE}$ | $\overline{EF}$ |
| 0 | 0 | 0 | 0 | H | H | L | L |
| 1 to n† | 1 to n† | 1 to n† | 1 to n† | H | H | L | H |
| (n + 1) to [512 – (m + 1)] | (n + 1) to [1024 – (m + 1)] | (n + 1) to [2048 – (m + 1)] | (n + 1) to [4096 – (m + 1)] | H | H | H | H |
| (512 – m)‡ to 511 | (1024 – m)‡ to 1023 | (2048 – m)‡ to 2047 | (4096 – m)‡ to 4095 | H | L | H | H |
| 512 | 1024 | 2048 | 4096 | L | L | H | H |

† n = empty offset (default value = 7)
‡ m = full offset (default value = 7)

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range, any input, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Continuous output current, $I_O$ . . . . . ±50 mA
Voltage applied to a disabled three-state output . . . . . 5.5 V
Storage temperature range under bias . . . . . −55°C to 125°C
Storage temperature range . . . . . −55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −2 | mA |
| $I_{OL}$ | Low-level output current | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2 mA | | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_I$ | Input current | $V_{CC}$ = 5.5 V, | $V_I = V_{CC}$ or 0 V | | | ±1 | µA |
| $I_{OZ}$ | High-impedance output current | $V_{CC}$ = 5.5 V, | $V_O = V_{CC}$ or 0 V | | | ±10 | µA |
| $C_i$‡ | Input capacitance | $V_I$ = 0 V, | f = 1 MHz | | | 10 | pF |
| $C_o$‡ | Output capacitance | $V_O$ = 0 V, | f = 1 MHz, | $\overline{OE} \geq V_{IH}$ | | 10 | pF |

‡ Specified by design but not tested

| PARAMETER | | TEST CONDITION | SN74ACT72211L $t_a$ = 15, 20, 25, 50 ns | | | SN74ACT72221L SN74ACT72231L SN74ACT72241L $t_a$ = 15, 25, 50 ns | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{CC}$ | Active supply current | $f_{clock}$ = 20 MHz | | | 140§ | | | 160¶ | mA |

§ $I_{CC}$ measurements are made with outputs open (only capacitive loading). Typical $I_{CC} = 65 + (f_{clock} \bullet 1.1/MHz) + (f_{clock} \bullet C_L \bullet 0.03/MHz\text{-}pF)$ mA ($C_L$ = external capacitive load)

¶ $I_{CC}$ measurements are made with outputs open (only capacitive loading). Typical $I_{CC} = 80 + (f_{clock} \bullet 2.1/MHz) + (f_{clock} \bullet C_L \bullet 0.03/MHz\text{-}pF)$ mA ($C_L$ = external capacitive load)

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | 'ACT72211L-15<br>'ACT72221L-15<br>'ACT72231L-15<br>'ACT72241L-15 | | 'ACT72211L-20 | | 'ACT72211L-25<br>'ACT72221L-25<br>'ACT72231L-25<br>'ACT72241L-25 | | 'ACT72211L-50<br>'ACT72221L-50<br>'ACT72231L-50<br>'ACT72241L-50 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency, RCLK or WCLK | | 66.7 | | 50 | | 40 | | 20 | MHz |
| $t_{cyc}$ | Clock cycle time, RCLK or WCLK | 15† | | 20 | | 25 | | 50 | | ns |
| $t_{w(CH)}$ | Pulse duration, RCLK or WCLK high | 6 | | 8 | | 10 | | 20 | | ns |
| $t_{w(CL)}$ | Pulse duration, RCLK or WCLK low | 6 | | 8 | | 10 | | 20 | | ns |
| $t_{w(RS)}$ | Pulse duration, $\overline{RS}$ low | 15 | | 20 | | 25 | | 50 | | ns |
| $t_{su(D)}$ | Setup time, D0–D8 before RCLK↑ | 4 | | 5 | | 6 | | 10 | | ns |
| $t_{su(EN)}$ | Setup time, $\overline{WEN1}$, WEN2‡, and $\overline{LD}$§ before WCLK↑; $\overline{REN1}$, $\overline{REN2}$, and $\overline{LD}$§ before RCLK↑ | 4 | | 5 | | 6 | | 10 | | ns |
| $t_{su(RS)}$ | Setup time, $\overline{REN1}$, $\overline{REN2}$, $\overline{WEN1}$, and WEN2/$\overline{LD}$ before $\overline{RS}$ high | 15 | | 20 | | 25 | | 50 | | ns |
| $t_{h(D)}$ | Hold time, D0–D8 after RCLK↑ | 1 | | 1 | | 1 | | 2 | | ns |
| $t_{h(EN)}$ | Hold time, $\overline{WEN1}$, WEN2‡, and $\overline{LD}$§ after WCLK↑; $\overline{REN1}$, $\overline{REN2}$, and $\overline{LD}$§ after RCLK↑ | 1 | | 1 | | 1 | | 2 | | ns |
| $t_{h(RS)}$ | Hold time, $\overline{REN1}$, $\overline{REN2}$, $\overline{WEN1}$, and WEN2/$\overline{LD}$ after $\overline{RS}$ high | 15 | | 20 | | 25 | | 50 | | |
| $t_{sk(1)}$ | Skew time between RCLK↑ and WCLK↑ to allow $\overline{EF}$ or $\overline{FF}$ to change logic levels during the current clock cycle | 6 | | 8 | | 10 | | 15 | | ns |
| $t_{sk(2)}$ | Skew time between RCLK↑ and WCLK↑ to allow $\overline{PAF}$ or $\overline{PAE}$ to change logic levels during the current clock cycle | 28 | | 35 | | 40 | | 45 | | ns |

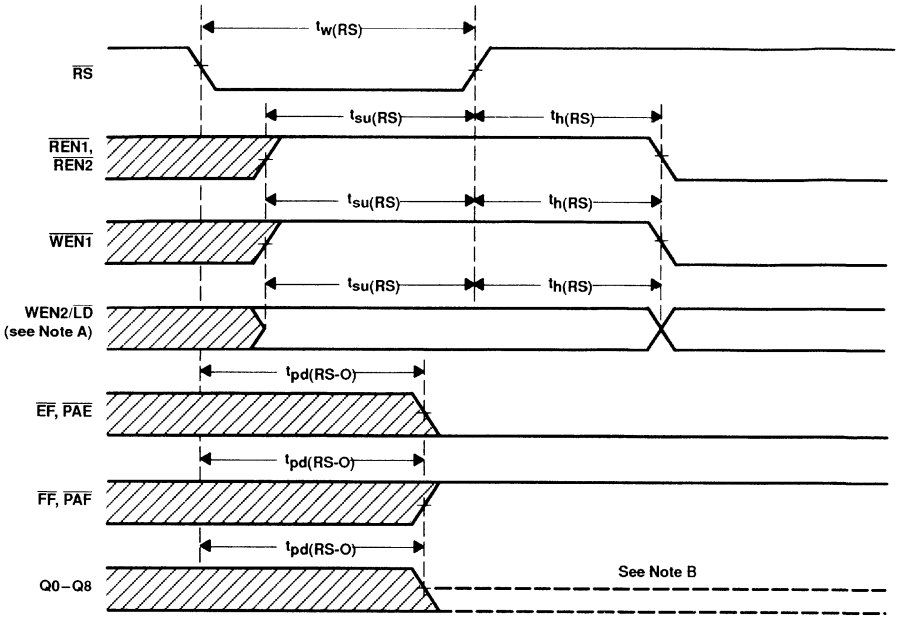
† Valid for $\overline{PAE}$ or $\overline{PAF}$ program values as follows:
≤ 63 bytes from the respective boundary for the SN74ACT72211L;
≤ 511 bytes from the respective boundary for the SN74ACT72221L/-72231L/-72241L;
minimum $t_{cyc}$ is 20 ns for program values greater than those indicated above.
‡ Applicable when the device is configured with two write-enable inputs (WEN2/$\overline{LD}$ = WEN2)
§ Applicable when the device is configured to have programmable flags (WEN2/$\overline{LD}$ = $\overline{LD}$)

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| | | 'ACT72211L-15<br>'ACT72221L-15<br>'ACT72231L-15<br>'ACT72241L-15 | | 'ACT72211L-20 | | 'ACT72211L-25<br>'ACT72221L-25<br>'ACT72231L-25<br>'ACT72241L-25 | | 'ACT72211L-50<br>'ACT72221L-50<br>'ACT72231L-50<br>'ACT72241L-50 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency, RCLK or WCLK | | 66.7 | | 50 | | 40 | | 20 | MHz |
| $t_a$ | Access time, RCLK↑ to Q0–Q8 valid | 2 | 10 | 2 | 12 | 3 | 15 | 3 | 25 | ns |
| $t_{pd(OE\text{-}Q)}$ | Propagation delay time, $\overline{OE}$ low to Q0–Q8 valid | 3 | 8 | 3 | 10 | 3 | 13 | 3 | 28 | ns |
| $t_{pd(R\text{-}EF)}$ | Propagation delay time, RCLK↑ to $\overline{EF}$ low or high | | 10 | | 12 | | 15 | | 30 | ns |
| $t_{pd(W\text{-}FF)}$ | Propagation delay time, WCLK↑ to $\overline{FF}$ low or high | | 10 | | 12 | | 15 | | 30 | ns |
| $t_{pd(R\text{-}AE)}$ | Propagation delay time, RCLK↑ to $\overline{PAE}$ low or high | | 10 | | 12 | | 15 | | 30 | ns |
| $t_{pd(W\text{-}AF)}$ | Propagation delay time, WCLK↑ to $\overline{PAF}$ low or high | | 10 | | 12 | | 15 | | 30 | ns |
| $t_{pd(RS\text{-}O)}$ | Propagation delay time, $\overline{RS}$ low to $\overline{FF}$ and $\overline{PAF}$ high and $\overline{EF}$, $\overline{PAE}$, and Q0–Q8 low | | 15 | | 20 | | 25 | | 50 | ns |
| $t_{en}$ | Enable time, $\overline{OE}$ low to Q0–Q8 at the low-impedance level† | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{dis}$ | Disable time, $\overline{OE}$ high to Q0–Q8 at the high-impedance level† | 3 | 8 | 3 | 10 | 3 | 13 | 3 | 28 | ns |

† These values are characterized but not tested.

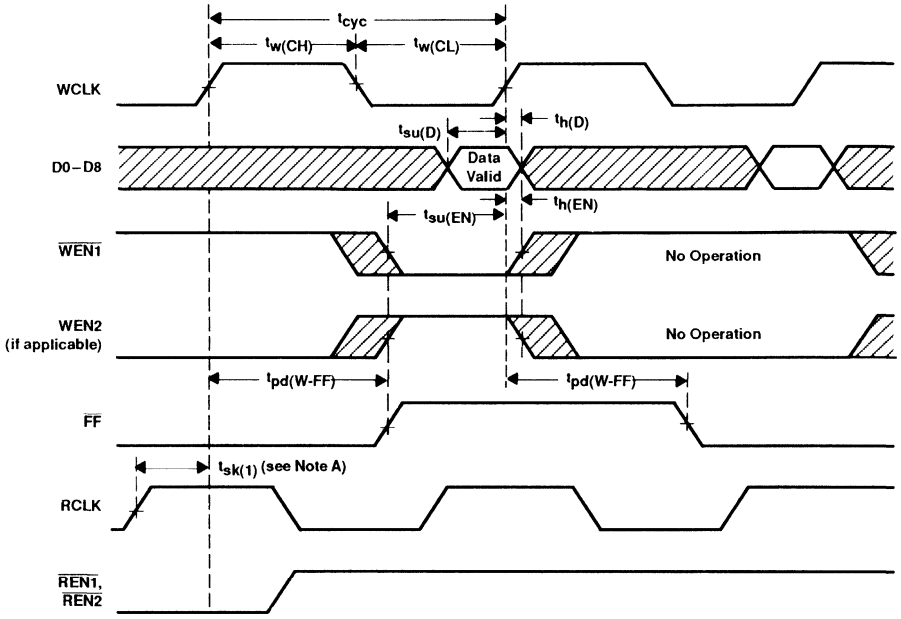
## timing diagrams




NOTES: A. Holding WEN2/$\overline{LD}$ high during reset makes the pin act as a second write-enable pin. Holding WEN2/$\overline{LD}$ low during reset makes the pin act as a load enable for the programmable flag offset registers.
B. After reset, the outputs are low if $\overline{OE}$ is low and at the high-impedance level if $\overline{OE}$ is high.
C. The clocks (RCLK, WCLK) can be free-running during reset.

**Figure 2. Reset Timing**

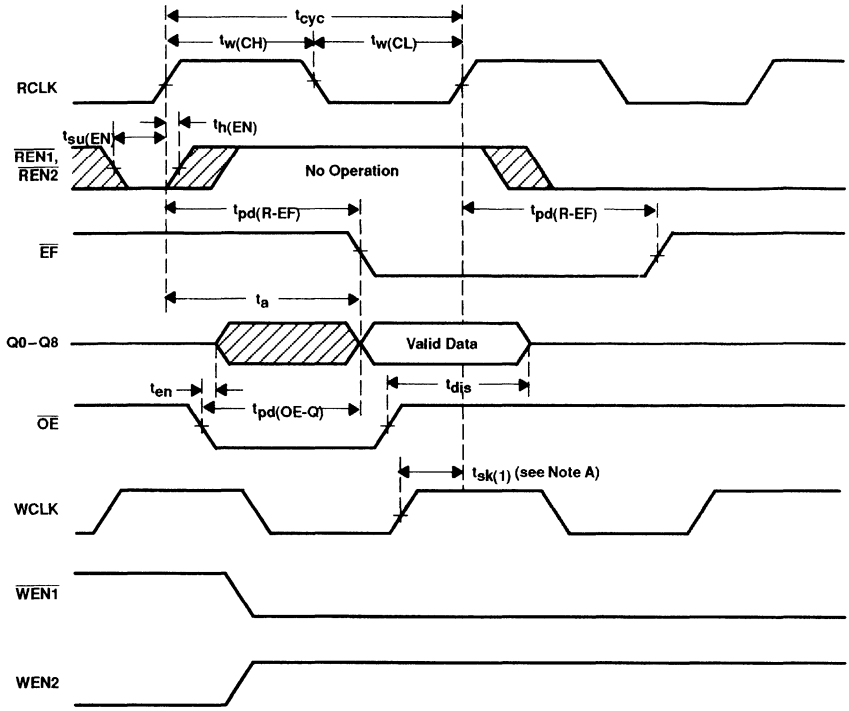
## timing diagrams (continued)




NOTES: A. $t_{sk(1)}$ is the minimum time between a rising RCLK edge and a subsequent rising WCLK edge for $\overline{FF}$ to change logic levels during the current clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than $t_{sk(1)}$, then $\overline{FF}$ may not change its logic level until the next WCLK rising edge.

**Figure 3. Write Cycle Timing**

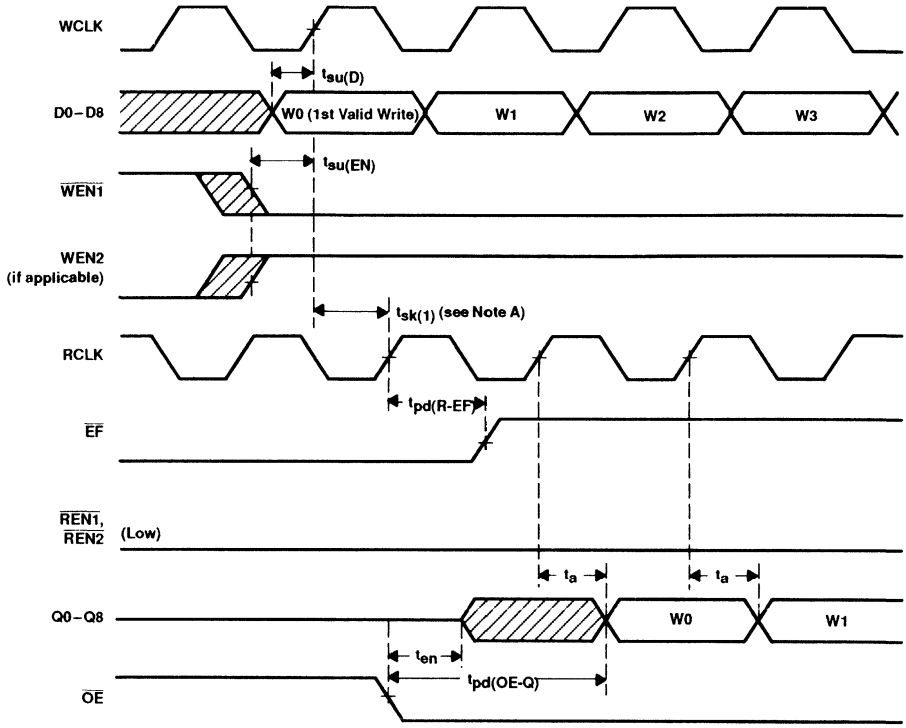
## timing diagrams (continued)




NOTES: A. $t_{sk(1)}$ is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change logic levels during the current clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than $t_{sk(1)}$, then $\overline{EF}$ may not change its logic level until the next RCLK rising edge.

**Figure 4. Read Cycle Timing**

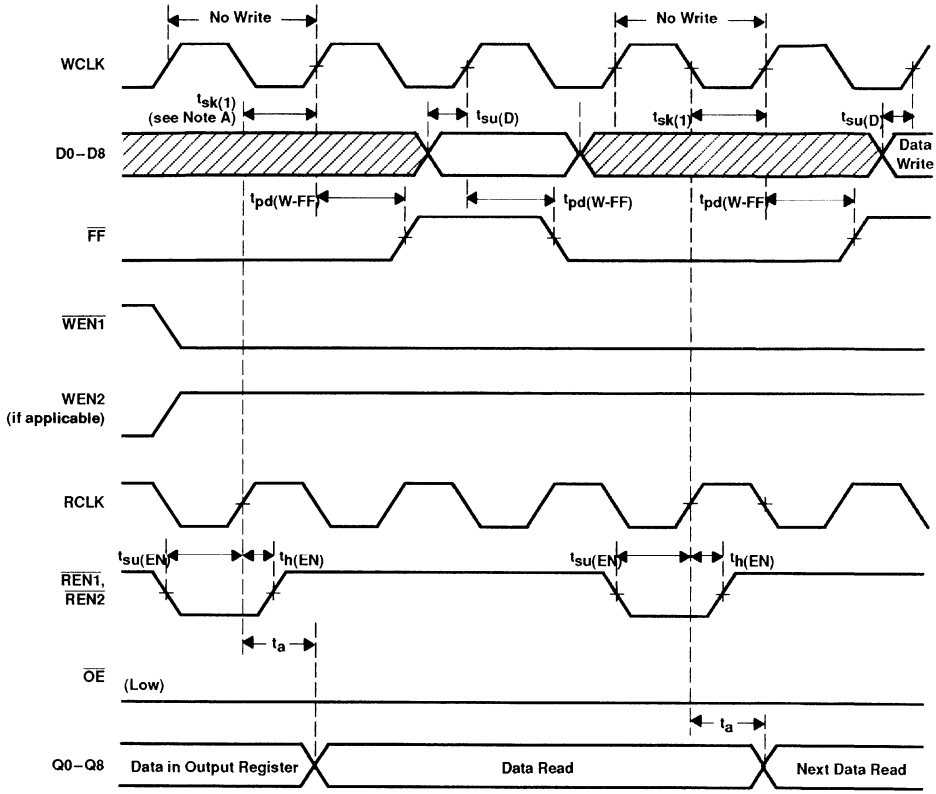
## timing diagrams (continued)




NOTES: A. $t_{sk(1)}$ is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than $t_{sk(1)}$, then $\overline{EF}$ may not change state until the next RCLK edge.

**Figure 5. First Data Word Latency Timing**

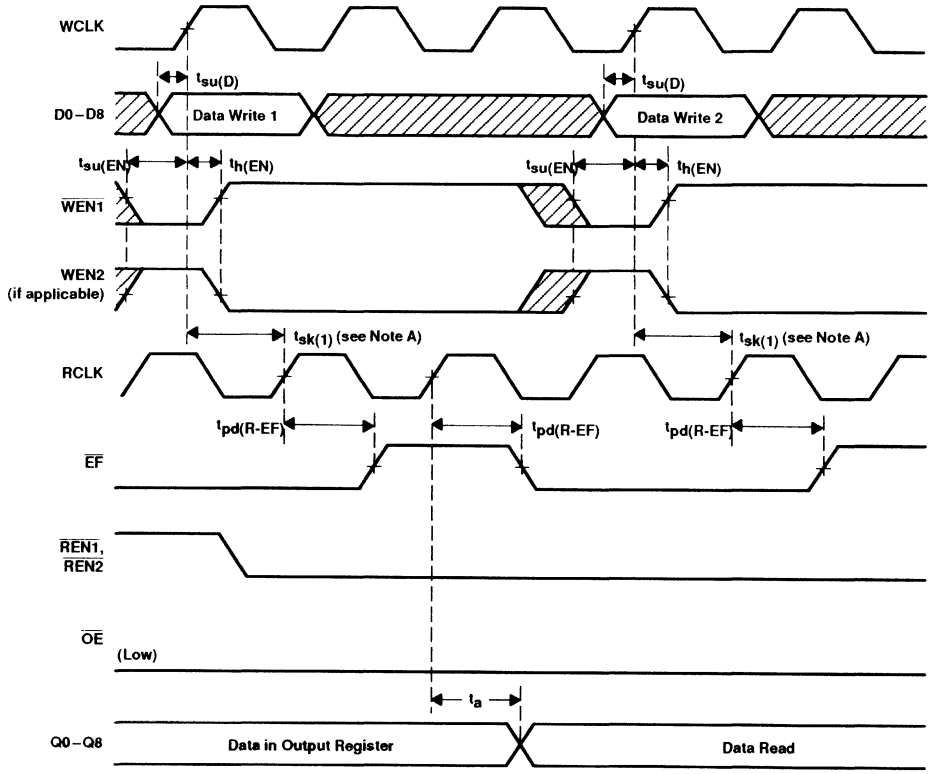
## timing diagrams (continued)




NOTES: A. $t_{sk(1)}$ is the minimum time between a rising RCLK edge and a subsequent rising WCLK edge for $\overline{FF}$ to change logic levels during the current clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than $t_{sk(1)}$, then $\overline{FF}$ may not change its logic level until the next WCLK rising edge.

**Figure 6. Full Flag Timing**

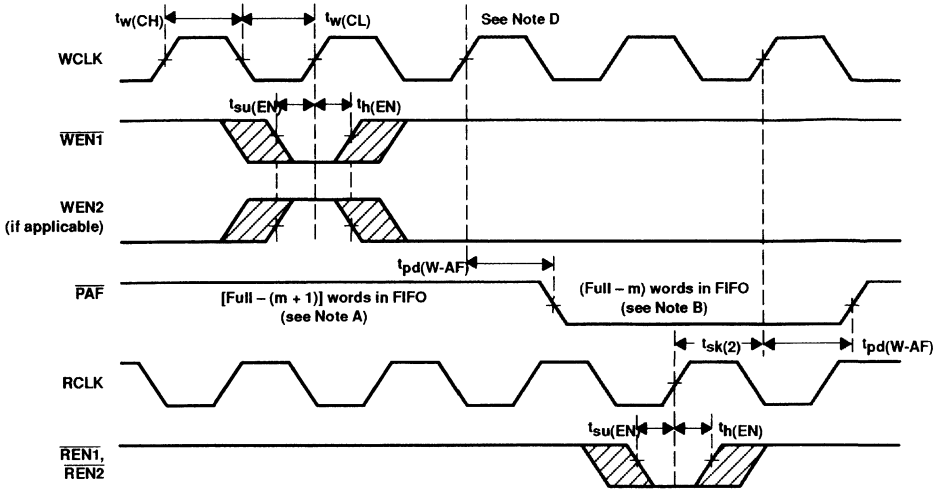
## timing diagrams (continued)




NOTES: A. $t_{sk(1)}$ is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change logic levels during the current clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than $t_{sk(1)}$, then $\overline{EF}$ may not change its logic level until the next RCLK rising edge.

**Figure 7. Empty Flag Timing**

## timing diagrams (continued)




NOTES: A. $\overline{PAF}$ offset = m

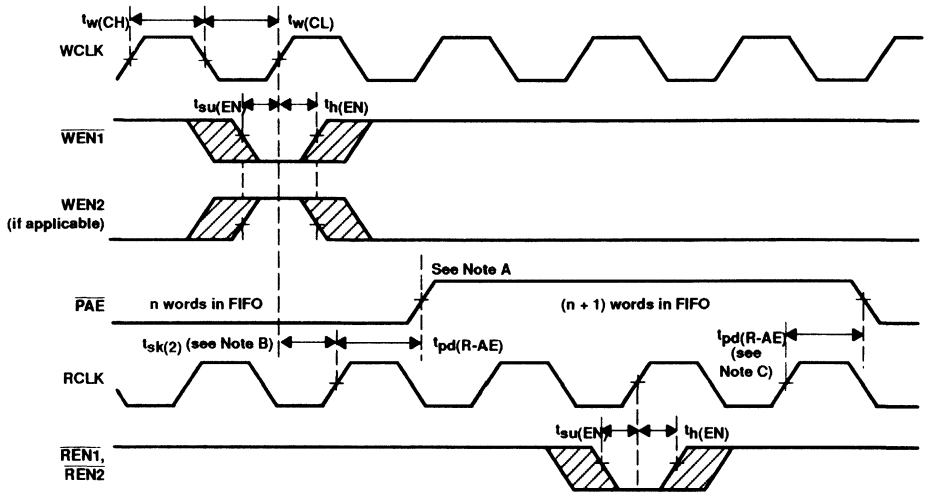
B. (512 – m) words for SN74ACT72211L, (1024 – m) words for SN74ACT72221L, (2048 – m) words for SN74ACT72231L, (4096 – m) words for SN74ACT72241L

C. $t_{sk(2)}$ is the minimum time between a rising RCLK edge and the subsequent rising WCLK edge for $\overline{PAF}$ to change its logic level during that clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than $t_{sk(2)}$, then $\overline{PAF}$ may not change its logic level until the next WCLK rising edge.

D. If a write is performed on this rising edge of the write clock, there will be [Full – (m – 1)] words in the FIFO when $\overline{PAF}$ goes low.

**Figure 8. Programmable Almost-Full Flag Timing**

## timing diagrams (continued)




NOTES: A. $\overline{PAE}$ offset = n

B. $t_{sk(2)}$ is the minimum time between a rising WCLK edge and the subsequent rising RCLK edge for $\overline{PAE}$ to change its logic level during that clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than $t_{sk(2)}$, then $\overline{PAE}$ may not change its logic level until the next RCLK rising edge.

C. If a write is performed on this rising edge of the write clock, there will be [Empty + (n – 1)] words in the FIFO when $\overline{PAE}$ goes low.

**Figure 9. Programmable Almost-Empty Flag Timing**

## timing diagrams (continued)

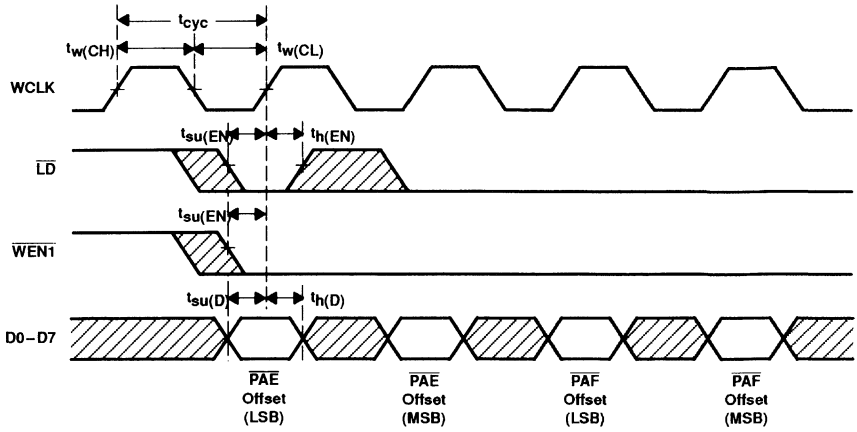



Figure 10. Write Offset Registers Timing

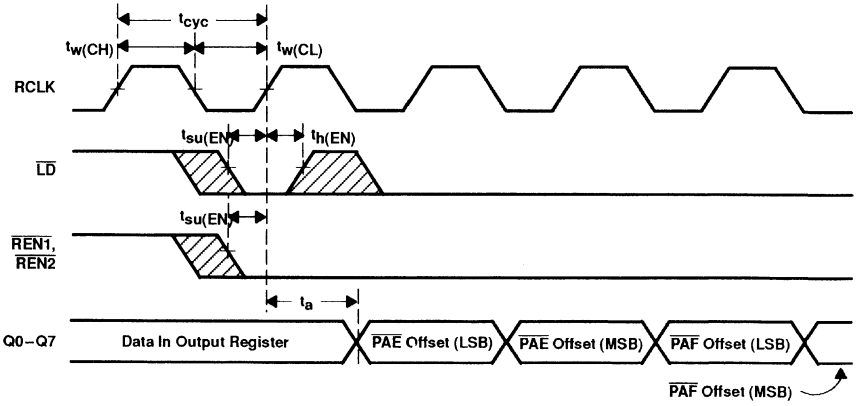



Figure 11. Read Offset Registers Timing

## PARAMETER MEASUREMENT INFORMATION

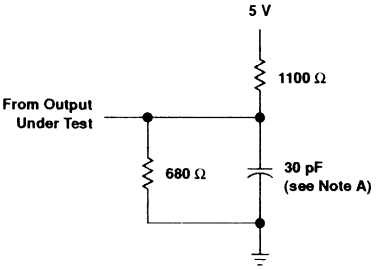



**Figure 12. Load Circuit**

NOTE A: Includes probe and jig capacitance

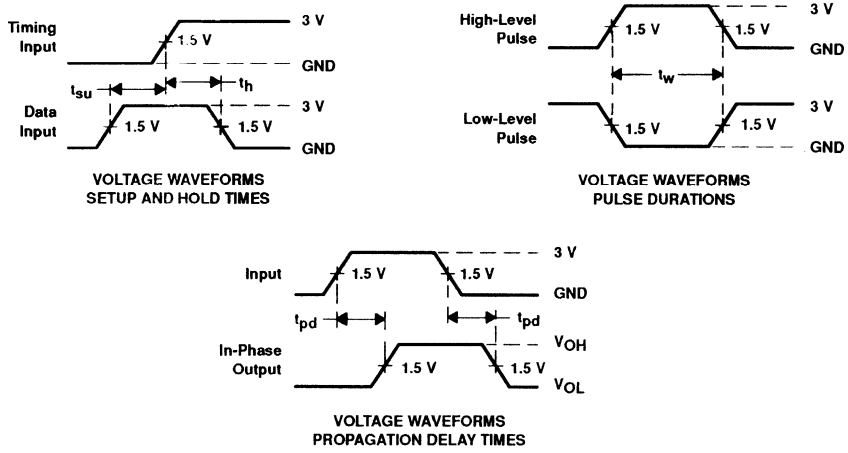



**Figure 13. Timing Reference Levels**

## APPLICATION INFORMATION

### width-expansion configuration

Word width is increased by connecting the corresponding input control signals of multiple devices. Composite empty and full flags should be created by monitoring all devices in width expansion. Almost-full and almost-empty status can be obtained from any one device. Figure 14 shows an 18-bit-wide data path formed by using two SN74ACT72211L/-72221L/-72231L/-72241L units.

In Figure 14, read enable 2 ($\overline{REN2}$) is grounded, and read enable 1 ($\overline{REN1}$) acts as the only read control. The write enable 2/load (WEN2/$\overline{LD}$) input of only one device is set low at reset to configure the device for programmable flags and to have the pin act as a load control for reading and writing the programmable flag offset registers.

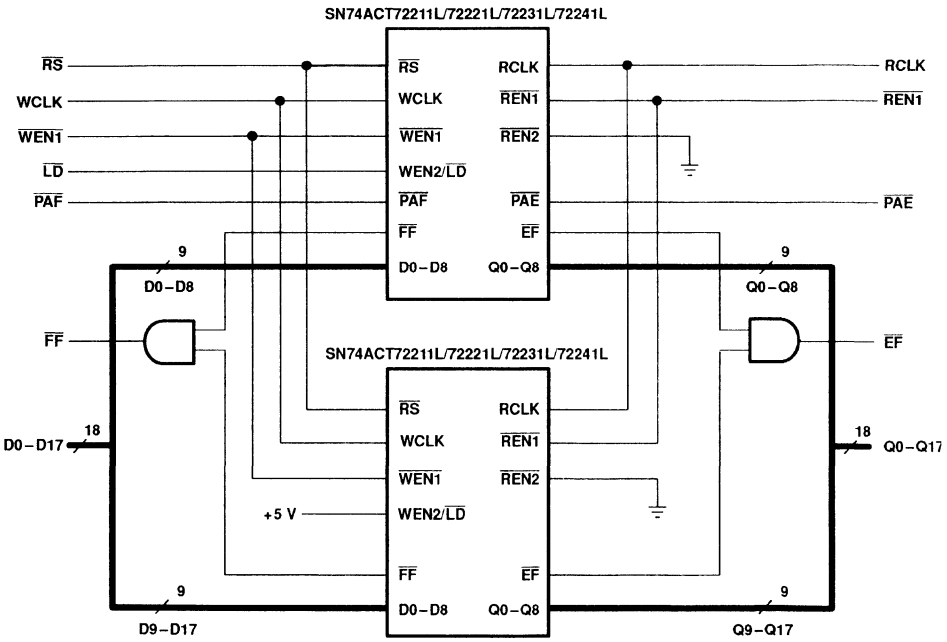
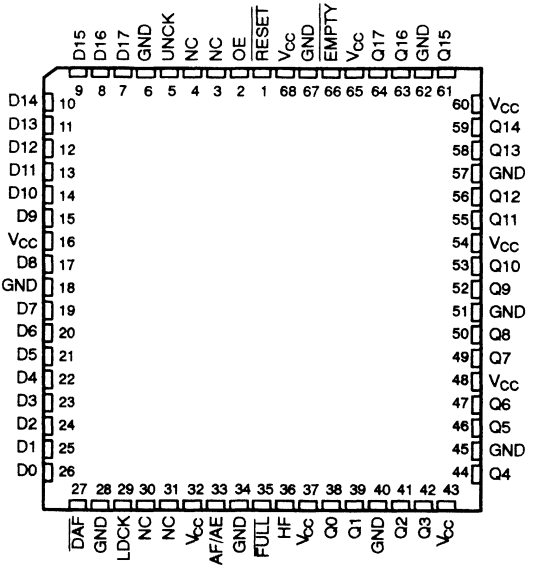



**Figure 14. Word-Width Expansion for 512 × 18/1024 × 18/2048 × 18/4096 × 18 FIFO**

SCAS187–D3599, AUGUST 1990–REVISED DECEMBER 1991

- Member of the Texas Instruments *Widebus*™ Family
- Independent Asynchronous Inputs and Outputs
- Low-Power Advanced CMOS Technology
- 1024 Words × 18 Bits
- Programmable Almost Full/Almost Empty Flag
- Empty, Full, and Half-Full Flags
- Fast Access Times of 15 ns With a 50-pF Load
- Fall-Through Time . . . 20 ns Typical
- Data Rates From 0 to 50 MHz
- High-Output Drive for Direct Bus Interface
- 3-State Outputs
- Available in 68-Pin PLCC (FN) Package

FN PACKAGE
(TOP VIEW)




NC–No internal connection

## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7802 is a 1024- by 18-bit FIFO for high-speed applications. It processes data in a bit-parallel format at rates up to 50 MHz and access times of 25 ns.

Data is written into the FIFO memory on a low-to-high transition on the load clock input (LDCK) and is read out on a low-to-high transition on the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 1024 the number of words clocked out. When the memory is full, LDCK has no effect on the data in the memory; when the memory is empty, UNCK has no effect.

Widebus is a trademark of Texas Instruments Incorporated.

## description (continued)

The FIFO memory status is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost full/almost empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full; the $\overline{EMPTY}$ output is low when the memory is empty. The HF output is high when the memory contains 512 or more words and low when it contains less than 512 words. The level of the AF/AE flag is determined by both the number of words in the FIFO and a user-definable offset X. AF/AE is high when the FIFO is almost full or almost empty, i.e., when it contains X or less words or (1024 – X) or more words. The almost full/almost empty offset value is either user-defined or the default value of 256; it is programmed during each reset cycle as follows:

***user-defined X:***

Step 1. Take $\overline{DAF}$ from high to low.
Step 2. If $\overline{RESET}$ is not already low, take $\overline{RESET}$ low.
Step 3. With $\overline{DAF}$ held low, take $\overline{RESET}$ high. This defines the AF/AE flag using X.

***default X:***

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.

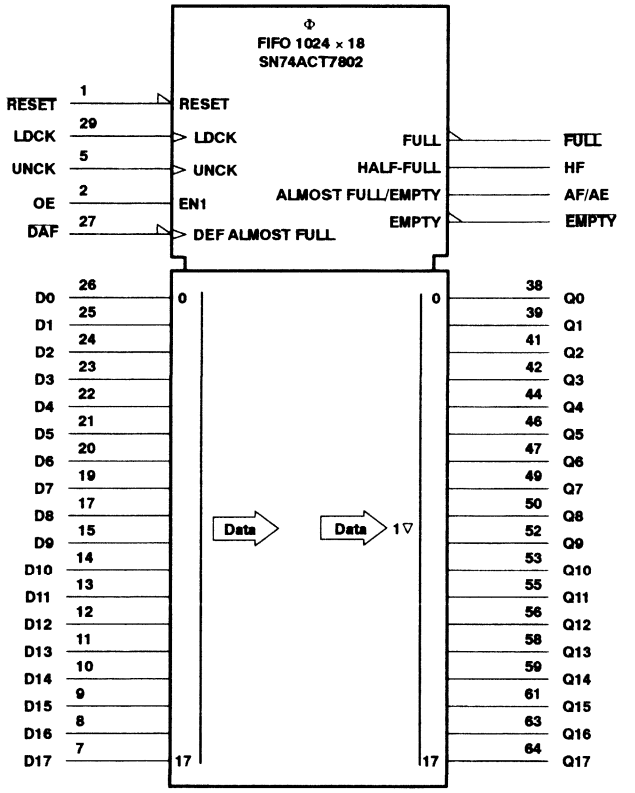
A low level on the reset ($\overline{RESET}$) input resets the FIFO internal clock stack pointers and sets $\overline{FULL}$ high, AF/AE high, HF low, and $\overline{EMPTY}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

The Q outputs are noninverting and are in the high-impedance state when the output-enable ($\overline{OE}$) input is low.

When writing to the FIFO after a reset pulse or when the FIFO is empty, the first active transition on LDCK drives $\overline{EMPTY}$ high and causes the first word written to the FIFO to appear on the Q outputs. Therefore, an active transition on UNCK is not required to read the first word written to the FIFO. Each subsequent read from the FIFO requires an active transition on UNCK.

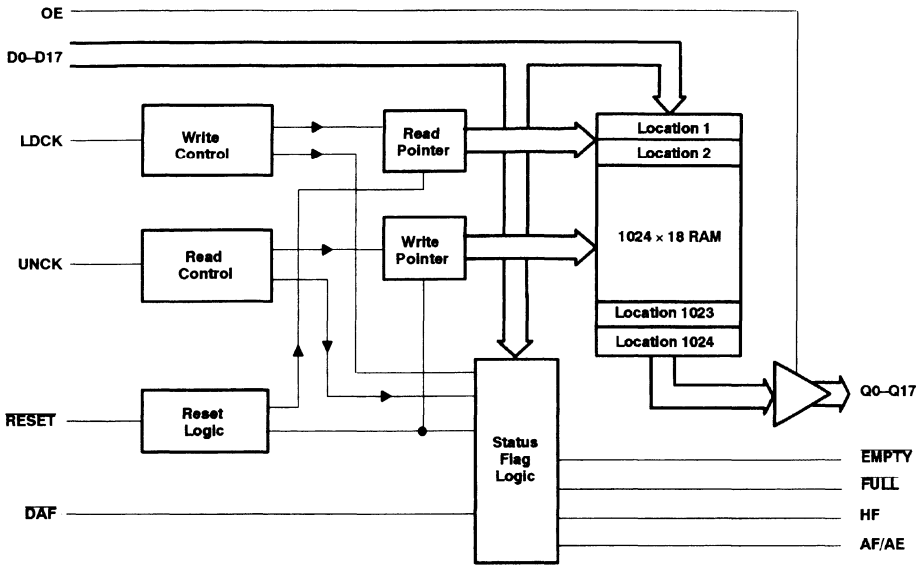
The SN74ACT7802 can be cascaded in the word-width direction but not in the word-depth direction.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

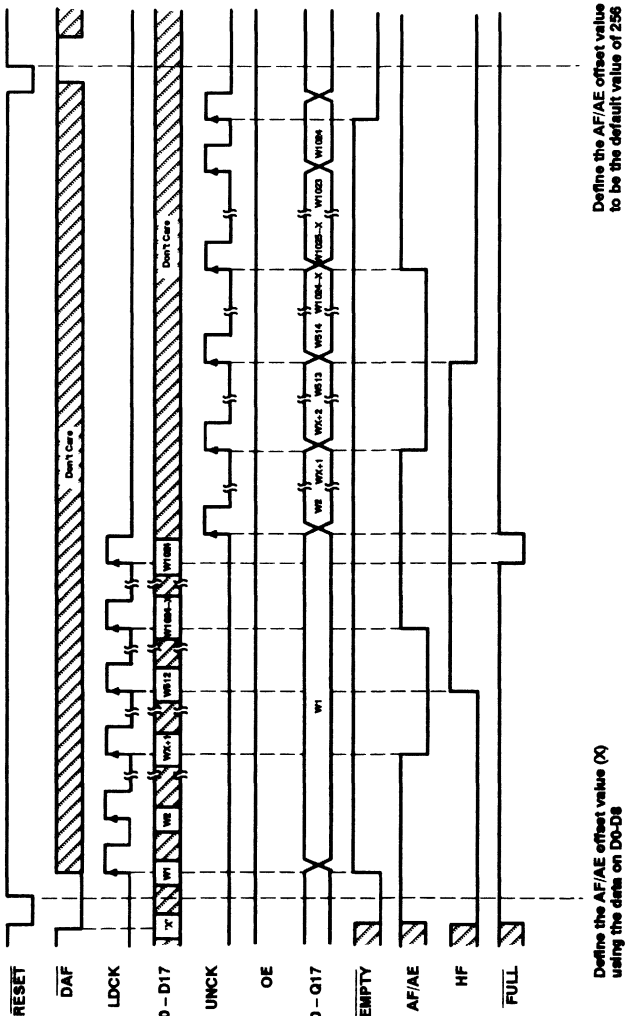
## functional block diagram






TEXAS INSTRUMENTS

timing diagram



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | 'ACT7802-20 | | 'ACT7802-30 | | 'ACT7802-40 | | 'ACT7802-60 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −8 | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | | | 16 | | 16 | | 16 | | 16 | mA |
| $f_{clock}$ | Clock frequency | | 50 | | 33 | | 25 | | 16.7 | | MHz |
| $t_w$ | Pulse duration | LDCK high | 8 | | 10 | | 14 | | 20 | | ns |
| | | LDCK low | 8 | | 10 | | 14 | | 20 | | |
| | | UNCK high | 8 | | 10 | | 14 | | 20 | | |
| | | UNCK low | 8 | | 10 | | 14 | | 20 | | |
| | | $\overline{DAF}$ high | 10 | | 10 | | 10 | | 10 | | |
| | | $\overline{RESET}$ low | 20 | | 20 | | 25 | | 25 | | |
| $t_{su}$ | Setup time | Data in (D0–D7) before LDCK↑ | 4 | | 4 | | 5 | | 5 | | ns |
| | | $\overline{RESET}$ inactive (high) before LDCK↑ | 5 | | 5 | | 5 | | 5 | | |
| | | Define AF/AE: D0–D8 before $\overline{DAF}$↓ | 5 | | 5 | | 5 | | 5 | | |
| | | Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑ | 7 | | 7 | | 7 | | 7 | | |
| | | Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑ | 5 | | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time | Data in (D0–D7) after LDCK↑ | 1 | | 1 | | 2 | | 2 | | ns |
| | | Define AF/AE: D0–D8 after $\overline{DAF}$↓ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑ | 0 | | 0 | | 0 | | 0 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 8 mA | | 2.4 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | | ±5 | μA |
| $I_{OZ}$ | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | | ±5 | μA |
| $I_{CC}$‡ | $V_I$ = $V_{CC}$ – 0.2 V or 0 | | | | | 400 | μA |
| $\Delta I_{CC}$‡ | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | $V_I$ = 0, | f = 1 MHz | | | 4 | | pF |
| $C_o$ | $V_O$ = 0, | f = 1 MHz | | | 8 | | pF |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (see Figures 4 and 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7802-20 | | | 'ACT7802-30 | | 'ACT7802-40 | | 'ACT7802-60 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK or UNCK | | 50 | | | 33 | | 25 | | 16.7 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | 8 | | 25 | 8 | 30 | 8 | 35 | 8 | 45 | ns |
| $t_{pd}$§ | UNCK↑ | Any Q | 12 | 21 | 25 | 12 | 30 | 12 | 35 | 12 | 45 | ns |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | 4 | | 16 | 4 | 18 | 4 | 20 | 4 | 22 | ns |
| $t_{PHL}$ | UNCK↑ | | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | |
| $t_{PHL}$ | $\overline{RESET}$↓ | $\overline{EMPTY}$ | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| $t_{PHL}$ | LDCK↑ | $\overline{FULL}$ | 4 | | 16 | 4 | 18 | 4 | 20 | 4 | 22 | ns |
| $t_{PLH}$ | UNCK↑ | FULL | 4 | | 15 | 4 | 17 | 4 | 19 | 4 | 21 | ns |
| | $\overline{RESET}$↓ | | 2 | | 15 | 2 | 17 | 2 | 19 | 2 | 21 | |
| $t_{pd}$ | LDCK↑ | AF/AE | 2 | | 18 | 2 | 20 | 2 | 22 | 2 | 24 | ns |
| | UNCK↑ | | 2 | | 18 | 2 | 20 | 2 | 22 | 2 | 24 | |
| $t_{PLH}$ | $\overline{RESET}$↓ | AF/AE | 2 | | 15 | 2 | 17 | 2 | 19 | 2 | 21 | ns |
| $t_{PLH}$ | LDCK↑ | HALF FULL | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| $t_{PHL}$ | UNCK↑ | HALF FULL | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| | $\overline{RESET}$↓ | | 2 | | 15 | 2 | 17 | 2 | 19 | 2 | 21 | |
| $t_{en}$ | OE | Any Q | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | ns |
| $t_{dis}$ | OE | Any Q | 2 | | 12 | 2 | 14 | 2 | 16 | 2 | 18 | ns |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ $I_{CC}$ tested with outputs open.
§ This parameter is measured with $C_L$ = 30 pF (see Figure 1).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| Cpd | Power dissipation capacitancer per channel | CL = 50 pF, | f = 5 MHz | 65 | pF |

## TYPICAL CHARACTERISTICS

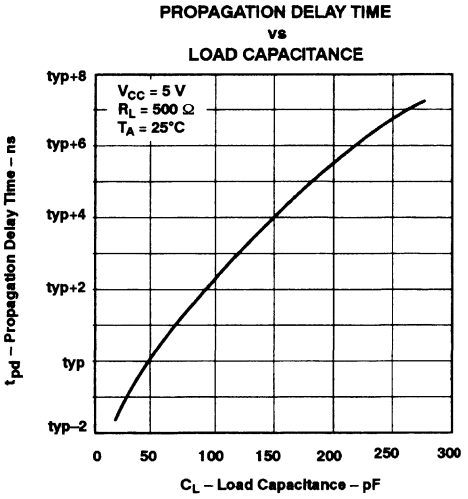



Figure 1

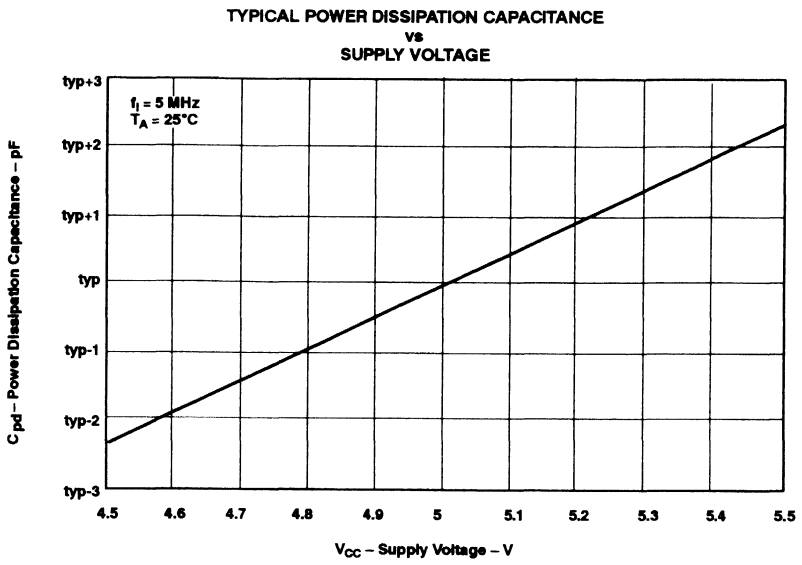



**Figure 2**

### calculating power dissipation

With $I_{CCF}$ taken from Figure 2, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## APPLICATION DATA

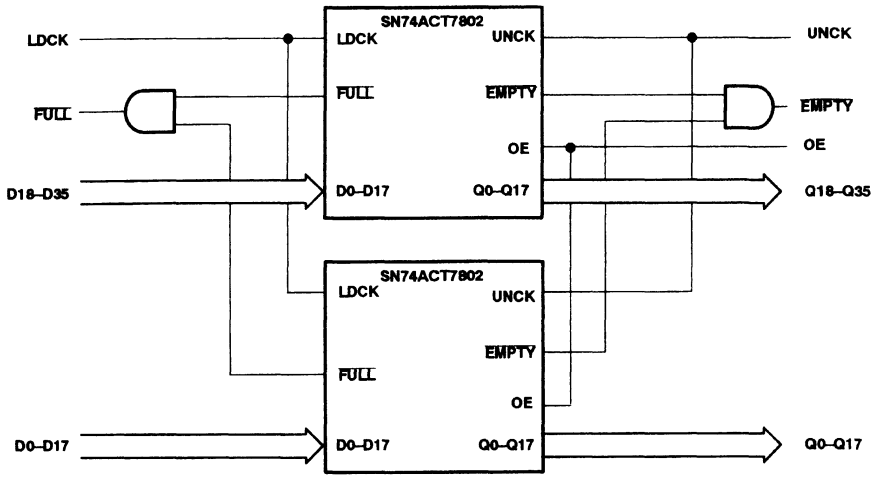



**Figure 3. Word-Width Expansion: 1024-Word by 36-Bit**

## PARAMETER MEASUREMENT INFORMATION

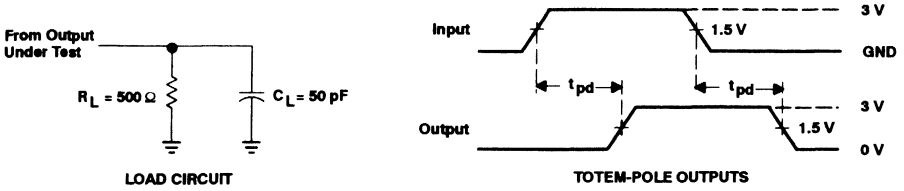
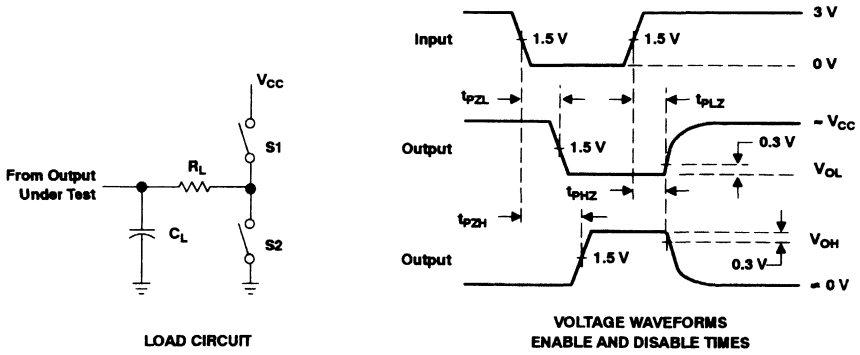



**Figure 4. Standard CMOS Outputs (FULL, HF, AF/AE, EMPTY)**




| PARAMETER | | $R_L$ | $C_L$† | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | – | 50 pF | Open | Open |

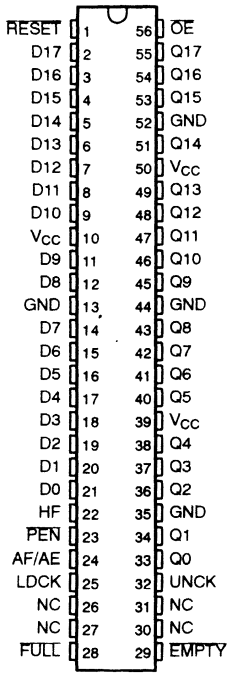
† Includes probe and test fixture capacitance.

**Figure 5. 3-State Outputs (Any Q)**

SCAS204–D4025, JUNE 1991–REVISED APRIL 1992

- **Member of the Texas Instruments *Widebus*™ Family**
- **Load Clock and Unload Clock May Be Asynchronous or Coincident**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**
- **512 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost Full/Almost Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7806 and SN74ACT7814**

DL PACKAGE
(TOP VIEW)




## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7804 is a 512-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 512. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost full/almost empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full and high when the memory is not full. The $\overline{EMPTY}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 256 or more words and is low when it contains 255 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{PEN}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words. The AF/AE flag is low when the FIFO contains between (X plus 1) and (511 minus Y) words.

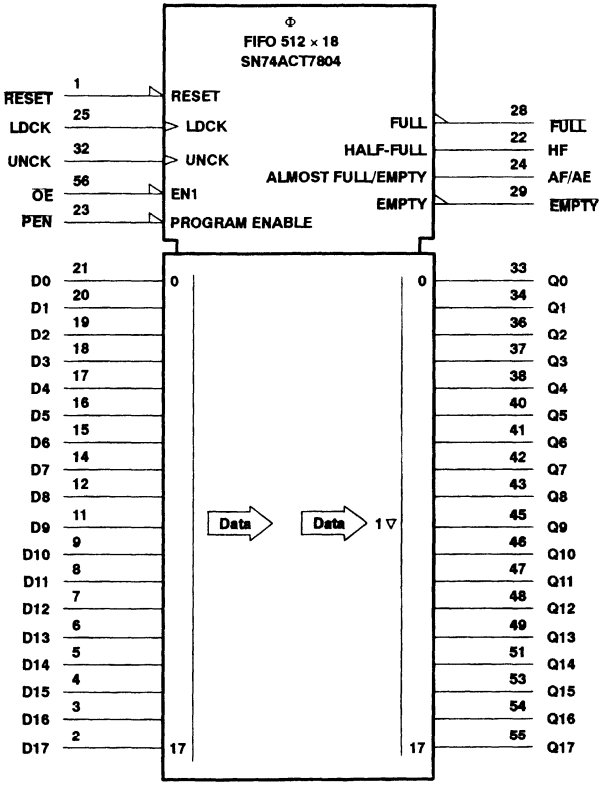
Widebus is a trademark of Texas Instruments Incorporated.

## description (continued)

A low level on the reset ($\overline{RESET}$) input resets the internal stack pointers and sets $\overline{FULL}$ high, AF/$\overline{AE}$ high, HF low, and $\overline{EMPTY}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

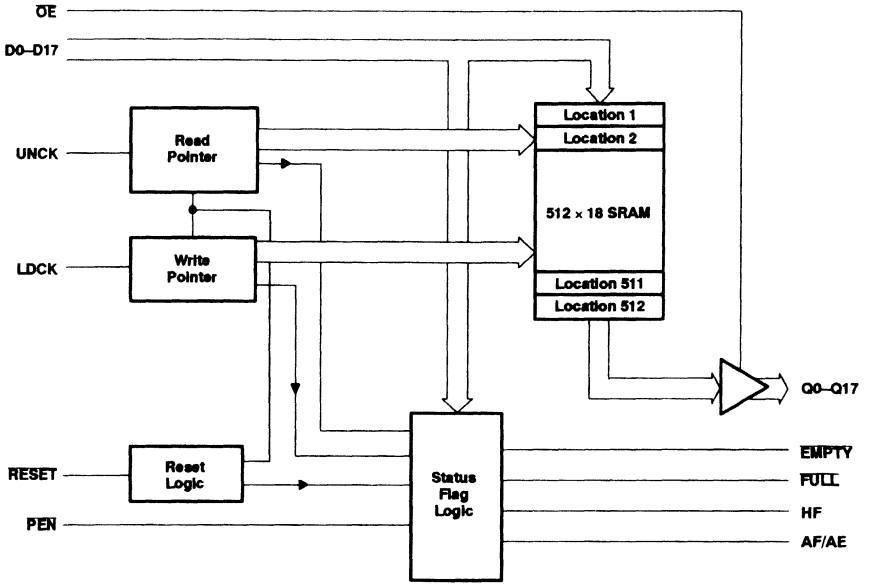
The first word loaded into empty memory causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{OE}$) input is high.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## functional block diagram



## Terminal Functions

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AF/AE | 24 | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 64 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (512 minus Y) or more words. AF/AE is high after reset. |
| D0–D17 | 21–14, 12–11, 9–2 | I | 18-bit data input port |
| $\overline{\text{EMPTY}}$ | 29 | O | Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low. |
| $\overline{\text{FULL}}$ | 28 | O | Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high. |
| HF | 22 | O | Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset. |
| LDCK | 25 | I | Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high. |
| $\overline{\text{OE}}$ | 56 | I | Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state. |
| $\overline{\text{PEN}}$ | 23 | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and LDCK is high. |
| Q0–Q17 | 33–34, 36–38, 40–43, 45–49, 51, 53–55 | O | 18-bit data output port |
| $\overline{\text{RESET}}$ | 1 | I | Reset. A low level on this input resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low. |
| UNCK | 32 | I | Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high. |

### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost empty offset value (X) and the almost full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words.

To program the offset values, $\overline{PEN}$ may be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of LDCK will reprogram Y to the binary value on D0–D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed.

A maximum value of 255 may be programmed for either X or Y. To use the default values of X = Y = 64, $\overline{PEN}$ must be held high.

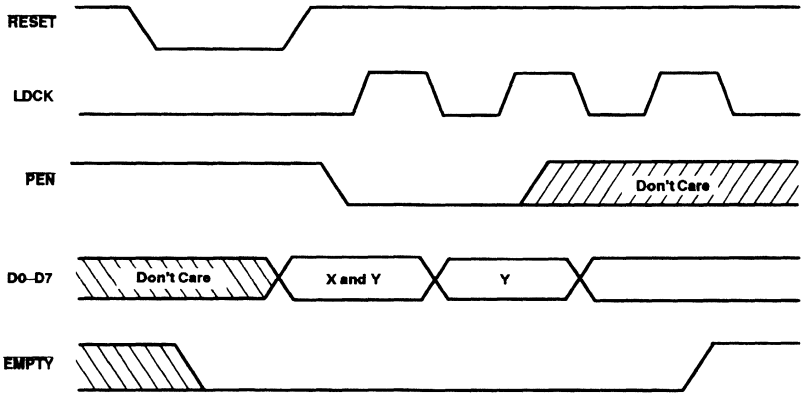
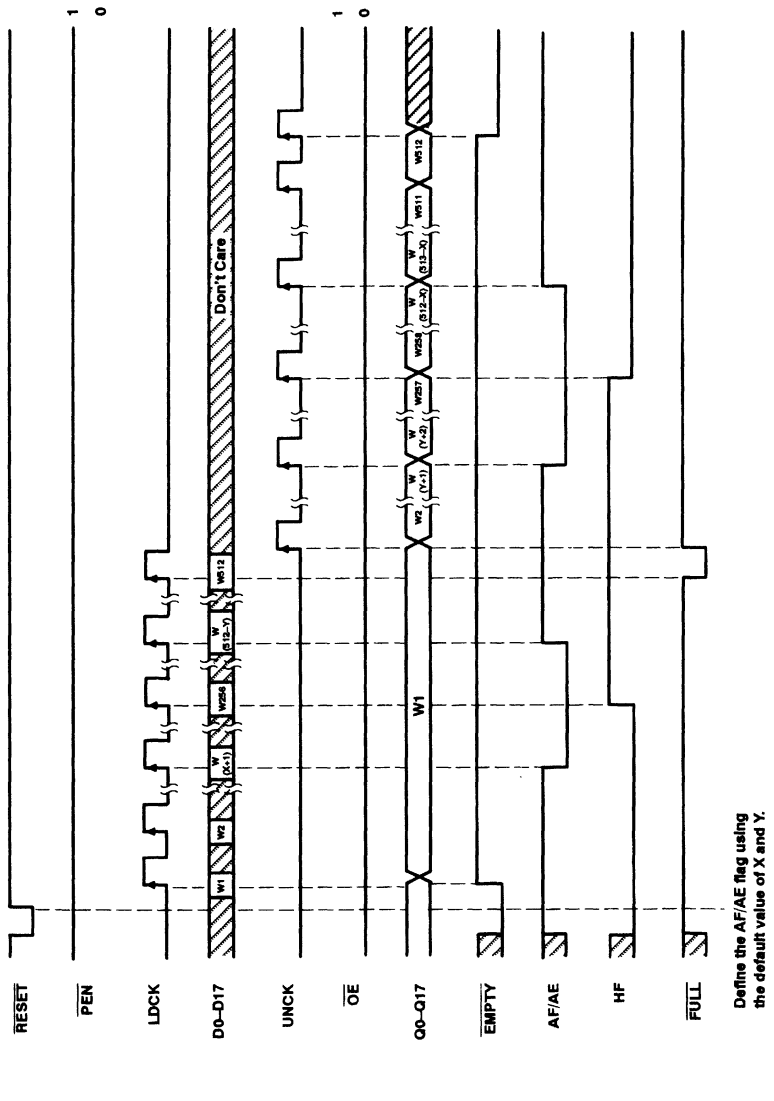



**Figure 1. Programming X and Y Separately**

## timing diagram






TEXAS INSTRUMENTS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | 'ACT7804-20 | | 'ACT7804-25 | | 'ACT7804-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, Flags | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | LDCK high or low | 7 | | 8 | | 12 | | ns |
| | | UNCK high or low | 7 | | 8 | | 12 | | |
| | | $\overline{PEN}$ low | 7 | | 8 | | 12 | | |
| | | $\overline{RESET}$ low | 10 | | 10 | | 12 | | |
| $t_{su}$ | Setup time | Data in (D0–D17) before LDCK↑ | 5 | | 5 | | 5 | | ns |
| | | $\overline{PEN}$ before LDCK↑ | 5 | | 5 | | 5 | | |
| | | LDCK inactive before $\overline{RESET}$ high | 5 | | 6 | | 6 | | |
| $t_h$ | Hold time | Data in (D0–D17) after LDCK↑ | 0 | | 0 | | 0 | | ns |
| | | LDCK inactive after $\overline{RESET}$ high | 5 | | 6 | | 6 | | |
| | | $\overline{PEN}$ low after LDCK↑ | 3 | | 3 | | 3 | | |
| | | $\overline{PEN}$ high after LDCK↓ | 0 | | 0 | | 0 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | µA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | 400 | µA |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 5 and 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7804-20 | | | 'ACT7804-25 | | 'ACT7804-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK or UNCK | | 50 | | | 40 | | 25 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | 9 | | 20 | 9 | 22 | 9 | 24 | ns |
| $t_{pd}$ | UNCK↑ | | 6 | 11.5 | 15 | 6 | 18 | 6 | 20 | |
| $t_{pd}$‡ | UNCK↑ | | | 10.5 | | | | | | |
| $t_{PLH}$ | LDCK↑ | EMPTY | 6 | | 15 | 6 | 17 | 6 | 19 | ns |
| $t_{PHL}$ | UNCK↑ | | 6 | | 15 | 6 | 17 | 6 | 19 | |
| $t_{PHL}$ | $\overline{RESET}$ low | | 4 | | 16 | 4 | 18 | 4 | 20 | |
| $t_{PHL}$ | LDCK↑ | FULL | 6 | | 15 | 6 | 17 | 6 | 19 | ns |
| $t_{PLH}$ | UNCK↑ | | 6 | | 15 | 6 | 17 | 6 | 19 | |
| $t_{PLH}$ | $\overline{RESET}$ low | | 4 | | 18 | 4 | 20 | 4 | 22 | |
| $t_{pd}$ | LDCK↑ | AF/AE | 7 | | 18 | 7 | 20 | 7 | 22 | ns |
| $t_{pd}$ | UNCK↑ | | 7 | | 18 | 7 | 20 | 7 | 22 | |
| $t_{PLH}$ | $\overline{RESET}$ low | | 2 | | 10 | 2 | 12 | 2 | 14 | |
| $t_{PLH}$ | LDCK↑ | HF | 5 | | 18 | 5 | 20 | 5 | 22 | ns |
| $t_{PHL}$ | UNCK↑ | | 7 | | 18 | 7 | 20 | 7 | 22 | |
| $t_{PHL}$ | $\overline{RESET}$ low | | 3 | | 12 | 3 | 14 | 3 | 16 | |
| $t_{en}$ | $\overline{OE}$ | Any Q | 2 | | 9 | 2 | 10 | 2 | 11 | ns |
| $t_{dis}$ | | | 2 | | 10 | 2 | 11 | 2 | 12 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This parameter is measured at $C_L$ = 30 pF (see Figure 3).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per FIFO channel | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | 53 | pF |

## APPLICATION INFORMATION

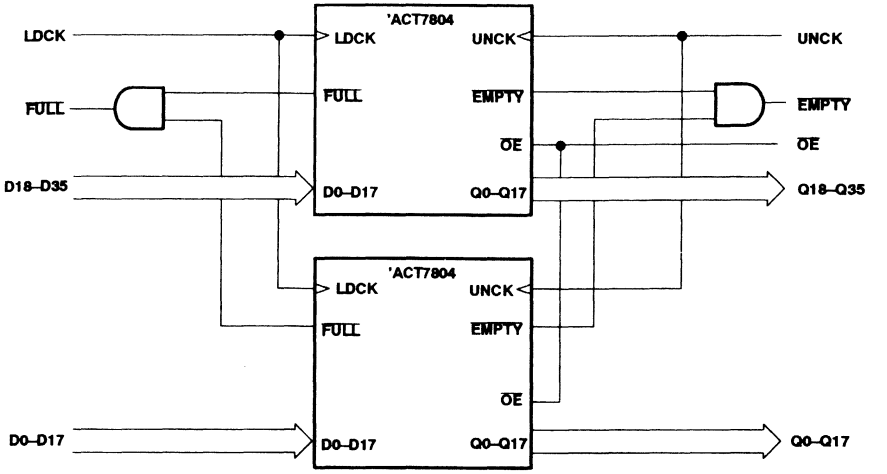



**Figure 2. Word-Width Expansion: 512 Words by 36 Bits**

## TYPICAL CHARACTERISTICS

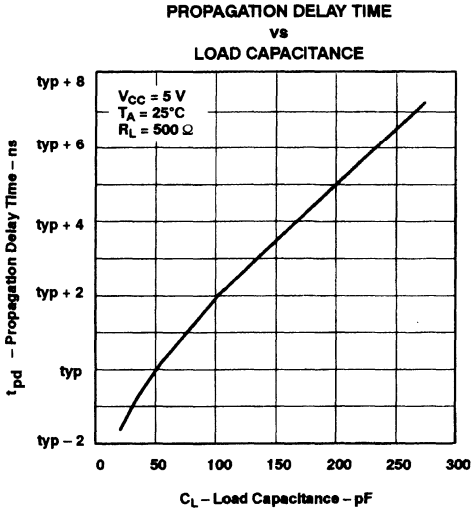



Figure 3

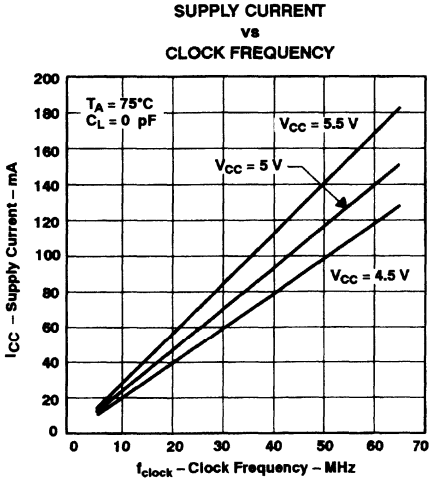



Figure 4



TEXAS INSTRUMENTS

### calculating power dissipation

With $I_{CCF}$ taken from Figure 4, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

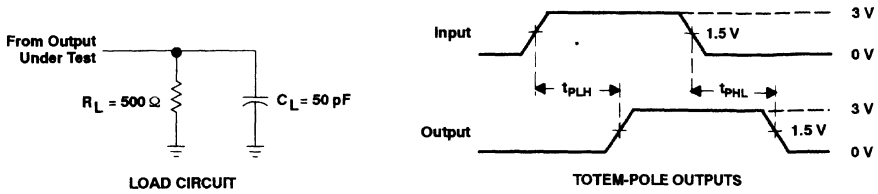
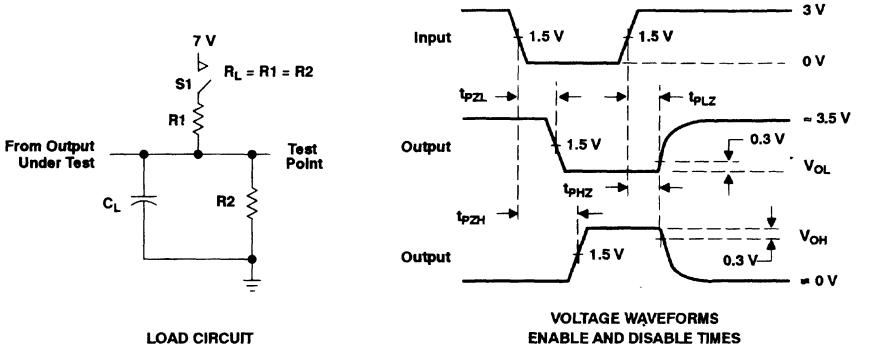



**Figure 5. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)**



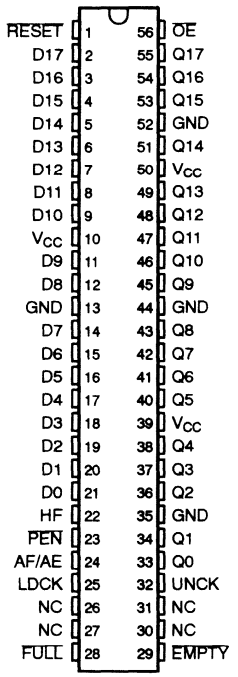

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

† Includes probe and test fixture capacitance.

**Figure 6. 3-State Outputs (Any Q)**

- **Member of the Texas Instruments *Widebus* ™ Family**
- **Load Clock and Unload Clock May Be Asynchronous or Coincident**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**
- **256 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost Full/Almost Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7804 and SN74ACT7814**

DL PACKAGE
(TOP VIEW)




## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7806 is a 256-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 256. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost full/almost empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 128 or more words and is low when it contains 127 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (256 minus Y) or more words. The AF/AE flag is low when the FIFO contains between (X plus 1) and (255 minus Y) words.

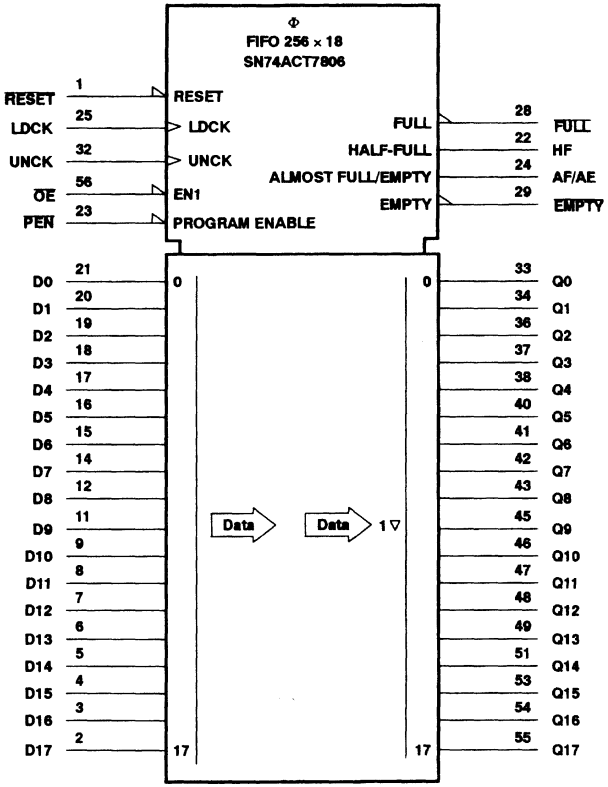
A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

Widebus is a trademark of Texas Instruments Incorporated.

## description (continued)

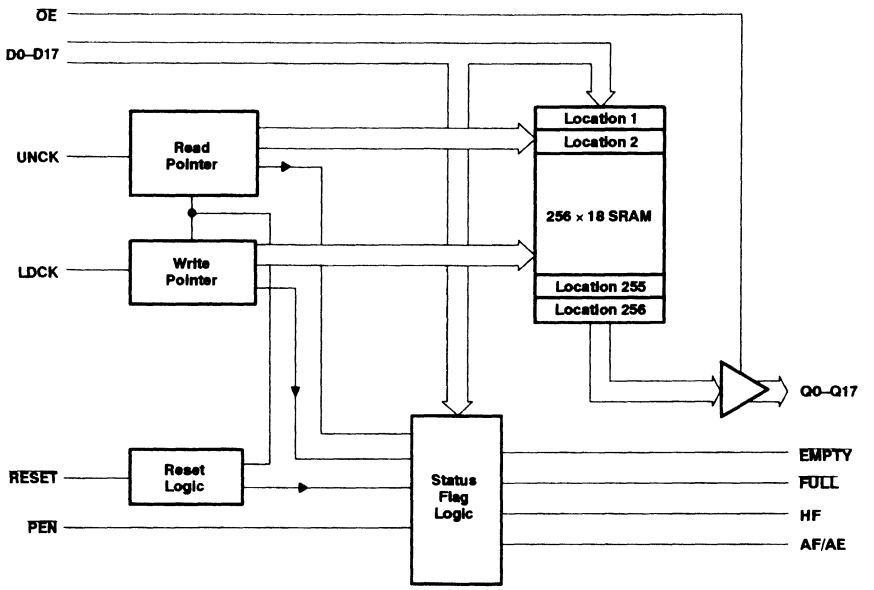
The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is high.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## functional block diagram



## Terminal Functions

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AF/AE | 24 | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 32 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (256 minus Y) or more words. AF/AE is high after reset. |
| D0–D17 | 21–14, 12–11, 9–2 | I | 18-bit data input port |
| $\overline{\text{EMPTY}}$ | 29 | O | Empty flag. $\overline{\text{EMPTY}}$ is high when the FIFO memory is not empty; $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty or upon assertion of $\overline{\text{RESET}}$. |
| $\overline{\text{FULL}}$ | 28 | O | Full flag. $\overline{\text{FULL}}$ is high when the FIFO memory is not full or upon assertion of $\overline{\text{RESET}}$; $\overline{\text{FULL}}$ is low when the FIFO memory is full. |
| HF | 22 | O | Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset. |
| LDCK | 25 | I | Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high. |
| $\overline{\text{OE}}$ | 56 | I | Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state. |
| $\overline{\text{PEN}}$ | 23 | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high. |
| Q0–Q17 | 33–34, 36–38, 40–43, 45–49, 51, 53–55 | O | 18-bit data output port |
| $\overline{\text{RESET}}$ | 1 | I | Reset. A low level on this input resets the FIFO and drives $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low. |
| UNCK | 32 | I | Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high. |

### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost empty offset value (X) and the almost full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag will be high when the FIFO contains X or less words or (256 minus Y) or more words.

To program the offset values, $\overline{PEN}$ may be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D6 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of LDCK will reprogram Y to the binary value on D0–D6 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed.

A maximum value of 127 may be programmed for either X or Y. To use the default values of X = Y = 32, $\overline{PEN}$ must be held high.

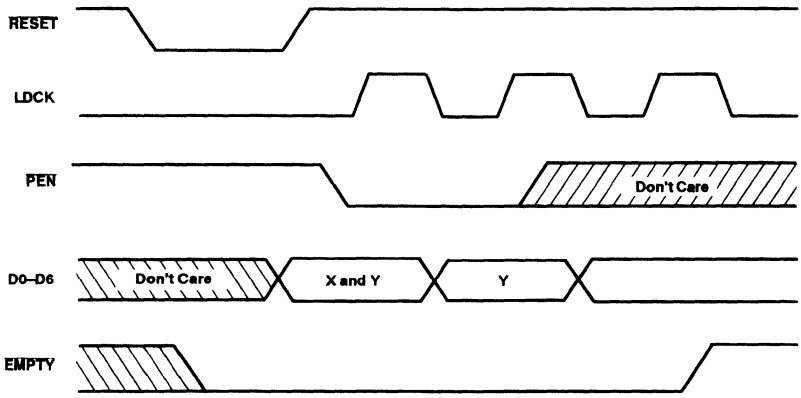
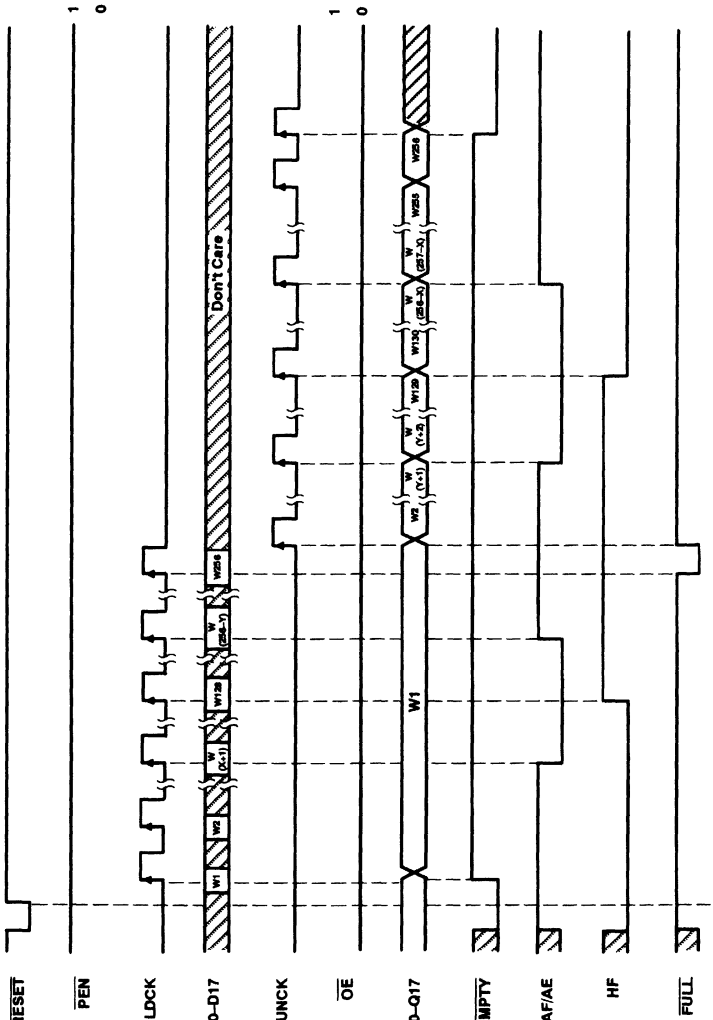



**Figure 1. Programming X and Y Separately**

## timing diagram






TEXAS INSTRUMENTS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | 'ACT7806-20 | | 'ACT7806-25 | | 'ACT7806-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | LDCK high or low | 7 | | 8 | | 12 | | ns |
| | | UNCK high or low | 7 | | 8 | | 12 | | |
| | | $\overline{PEN}$ low | 7 | | 8 | | 12 | | |
| | | $\overline{RESET}$ low | 10 | | 10 | | 12 | | |
| $t_{su}$ | Setup time | Data in (D0–D17) before LDCK↑ | 5 | | 5 | | 5 | | ns |
| | | $\overline{PEN}$ before LDCK↑ | 5 | | 5 | | 5 | | |
| | | LDCK inactive before $\overline{RESET}$ high | 5 | | 6 | | 6 | | |
| $t_h$ | Hold time | Data in (D0–D17) after LDCK↑ | 0 | | 0 | | 0 | | ns |
| | | LDCK inactive after $\overline{RESET}$ high | 5 | | 6 | | 6 | | |
| | | $\overline{PEN}$ low after LDCK↑ | 3 | | 3 | | 3 | | |
| | | $\overline{PEN}$ high after LDCK↓ | 0 | | 0 | | 0 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | µA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | 400 | µA |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 5 and 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7806-20 | | | 'ACT7806-25 | | 'ACT7806-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK or UNCK | | 50 | | | 40 | | 25 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | 9 | | 20 | 9 | 22 | 9 | 24 | ns |
| $t_{pd}$ | UNCK↑ | | 6 | 11.5 | 15 | 6 | 18 | 6 | 20 | |
| $t_{pd}$‡ | UNCK↑ | | | 10.5 | | | | | | |
| $t_{PLH}$ | LDCK↑ | EMPTY | 6 | | 15 | 6 | 17 | 6 | 19 | ns |
| $t_{PHL}$ | UNCK↑ | | 6 | | 15 | 6 | 17 | 6 | 19 | |
| $t_{PHL}$ | $\overline{RESET}$ low | | 4 | | 16 | 4 | 18 | 4 | 20 | |
| $t_{PHL}$ | LDCK↑ | FULL | 6 | | 15 | 6 | 17 | 6 | 19 | ns |
| $t_{PLH}$ | UNCK↑ | | 6 | | 15 | 6 | 17 | 6 | 19 | |
| $t_{PLH}$ | $\overline{RESET}$ low | | 4 | | 18 | 4 | 20 | 4 | 22 | |
| $t_{pd}$ | LDCK↑ | AF/AE | 7 | | 18 | 7 | 20 | 7 | 22 | ns |
| $t_{pd}$ | UNCK↑ | | 7 | | 18 | 7 | 20 | 7 | 22 | |
| $t_{PLH}$ | $\overline{RESET}$ low | | 2 | | 10 | 2 | 12 | 2 | 14 | |
| $t_{PLH}$ | LDCK↑ | HF | 5 | | 18 | 5 | 20 | 5 | 22 | ns |
| $t_{PHL}$ | UNCK↑ | | 7 | | 18 | 7 | 20 | 7 | 22 | |
| $t_{PHL}$ | $\overline{RESET}$ low | | 3 | | 12 | 3 | 14 | 3 | 16 | |
| $t_{en}$ | $\overline{OE}$ | Any Q | 2 | | 9 | 2 | 10 | 2 | 11 | ns |
| $t_{dis}$ | | | 2 | | 10 | 2 | 11 | 2 | 12 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This parameter is measured at $C_L$ = 30 pF (see Figure 3).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per FIFO channel | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | 53 | pF |

## APPLICATION INFORMATION

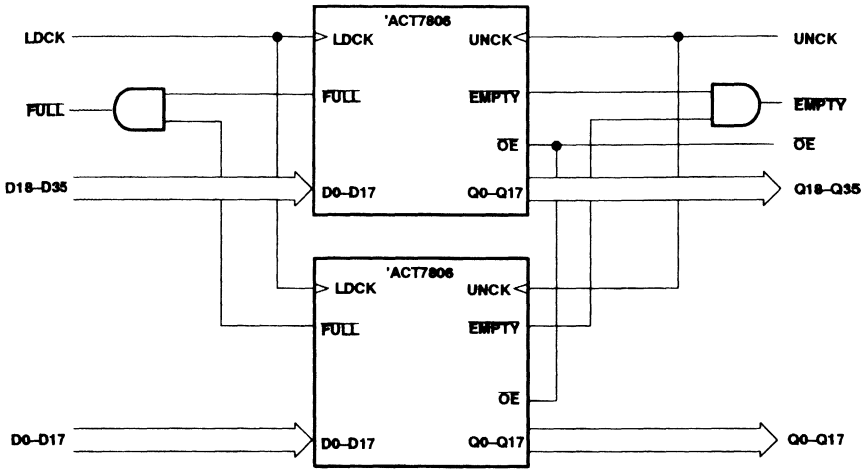



**Figure 2. Word-Width Expansion: 256 Words by 36 Bits**

## TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

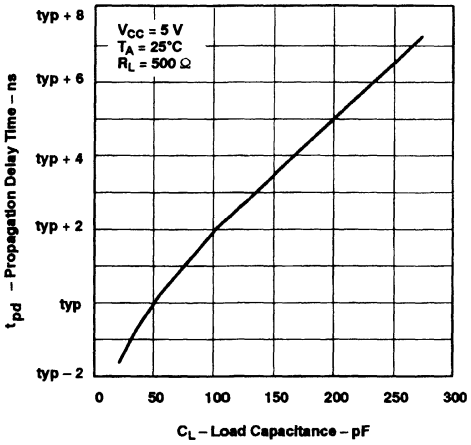



Figure 3

SUPPLY CURRENT
vs
CLOCK FREQUENCY

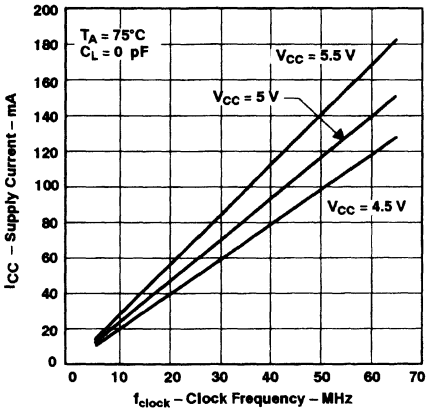



Figure 4



TEXAS INSTRUMENTS

### calculating power dissipation

With $I_{CCF}$ taken from Figure 4, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

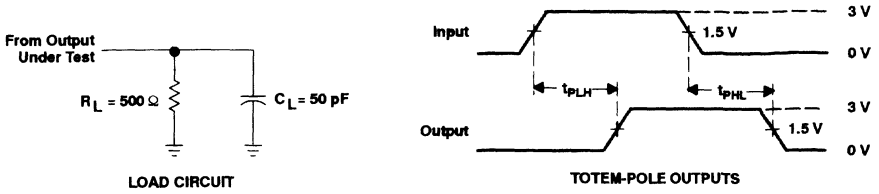
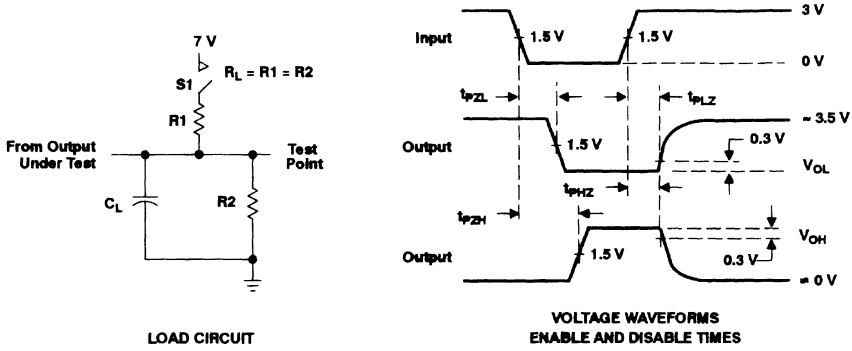



Figure 5. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)




| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

† Includes probe and test fixture capacitance.

Figure 6. 3-State Outputs (Any Q)

SCAS205–D4026, FEBRUARY 1991–REVISED APRIL 1992

- **Load Clocks and Unload Clocks May Be Asynchronous or Coincident**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Fast Access Times of 15 ns With a 50-pF Load**
- **Programmable Almost Full/Almost Empty Flag**
- **Expansion Logic for Depth Cascading**
- **Empty, Full, and Half-Full Flags**
- **Fall-Through Time of 20 ns Typ**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Available in 44-Pin PLCC (FN) or Space-Saving 64-Pin Shrink Quad Flat Pack (PM)**

## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7808 is a 2048-word by 9-bit FIFO designed for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 2048. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

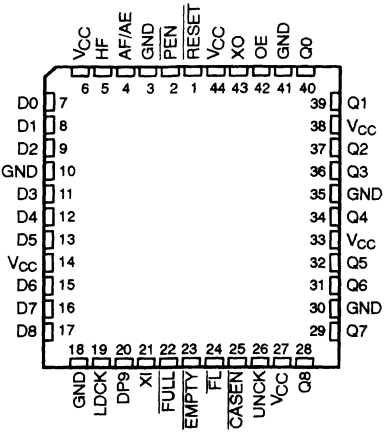
Status of the FIFO memory is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost full/almost empty (AF/$\overline{AE}$) flags. The $\overline{FULL}$ output is low when the memory is full and high when the memory is not full. The $\overline{EMPTY}$ output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 1024 or more words and is low when it contains 1023 or less words. The AF/$\overline{AE}$ status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset may be used to program the almost empty offset value (X) and the almost full offset value (Y) if program enable ($\overline{PEN}$) is low. The AF/$\overline{AE}$ flag is high when the FIFO contains X or less words or (2048 minus Y) or more words. The AF/$\overline{AE}$ flag is low when the FIFO contains between (X + 1) and (2047 minus Y) words.

A low level on the reset ($\overline{RESET}$) input resets the internal stack pointers and sets $\overline{FULL}$ high, AF/$\overline{AE}$ high, HF low, and $\overline{EMPTY}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

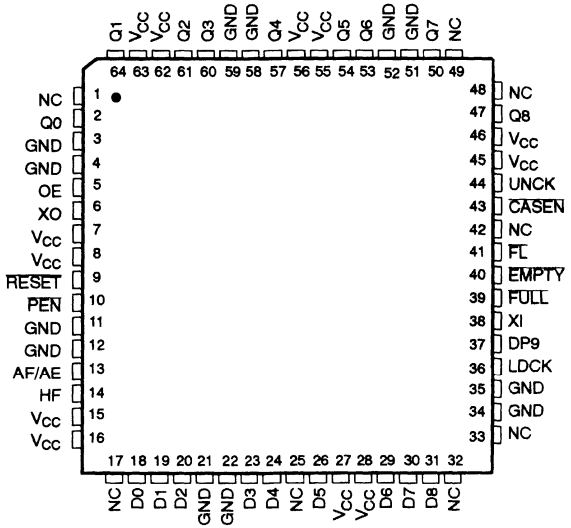
The first word loaded into empty memory causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{OE}$) input is low. $\overline{OE}$ does not affect the output flags.

Cascading is easily accomplished in the word-width and word-depth directions. When not using the FIFO in depth expansion, cascade enable ($\overline{CASEN}$) must be tied high.

**FN PACKAGE**
**(TOP VIEW)**




**PM PACKAGE**
**(TOP VIEW)**

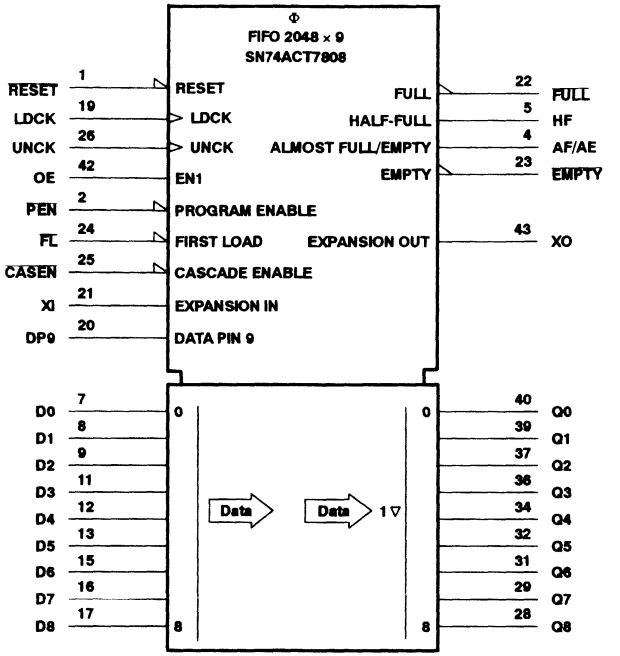



NC – No internal connection



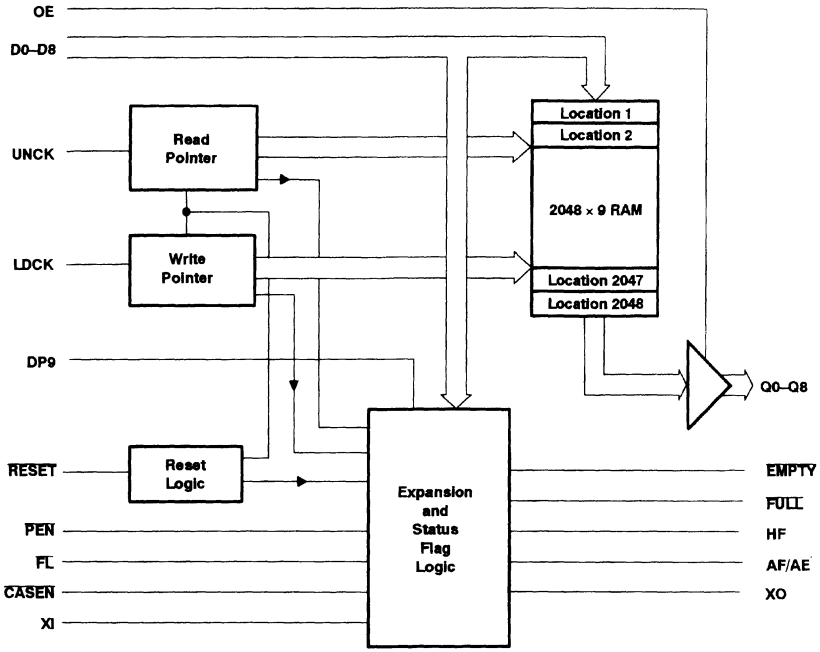
TEXAS INSTRUMENTS

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

## functional block diagram






TEXAS INSTRUMENTS

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| AF/AE | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 256 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (2048 minus Y) or more words. AF/AE is high after reset. |
| $\overline{\text{CASEN}}$† | I | Cascade enable. When multiple 'ACT7808 devices are depth cascaded, every device must have its $\overline{\text{CASEN}}$ input tied low. $\overline{\text{CASEN}}$ must be tied high when a device is not used in depth expansion. |
| D0–D8 | I | 9-bit data input port |
| DP9 | I | DP9 is used as the most significant bit when programming the AF/AE offset values. |
| $\overline{\text{EMPTY}}$ | O | Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low. |
| $\overline{\text{FL}}$† | I | When multiple 'ACT7808 devices are depth cascaded, the first device in the chain must have its $\overline{\text{FL}}$ input tied low, and all other devices must have their $\overline{\text{FL}}$ inputs tied high. |
| $\overline{\text{FULL}}$ | O | Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high. |
| HF | O | Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset. |
| LDCK | I | Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high. |
| OE | I | Output enable. When OE is low, the data outputs are in the high-impedance state. |
| $\overline{\text{PEN}}$ | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and LDCK is high. |
| Q0–Q8 | O | 9-bit data output port |
| $\overline{\text{RESET}}$ | I | Reset. A low level on this input resets the FIFO and drives $\overline{\text{FULL}}$ and AF/AE high and HF and $\overline{\text{EMPTY}}$ low. |
| UNCK | I | Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high. |
| XI† | I | Expansion input (XI) and expansion output (XO). When multiple 'ACT7808 devices are depth cascaded, the XO of one device must be connected to the XI of the next device in the chain. The XO of the last device in the chain is connected to the XI of the first device in the chain. |
| XO† | O | |

† See Figures 2 and 3 for application information on FIFO word-width and depth expansions, respectively.

### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost-empty offset value (X) and the almost-full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or less words or (2048 minus Y) or more words.

To program the offset values, $\overline{PEN}$ may be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D8 and DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D8 and DP9 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed.

A maximum value of 1023 may be programmed for either X or Y. To use the default values of X = Y = 256, $\overline{PEN}$ must be held high.

### timing diagram

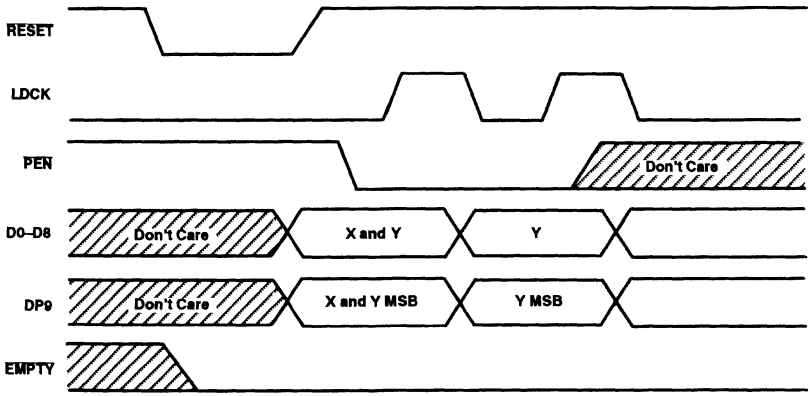
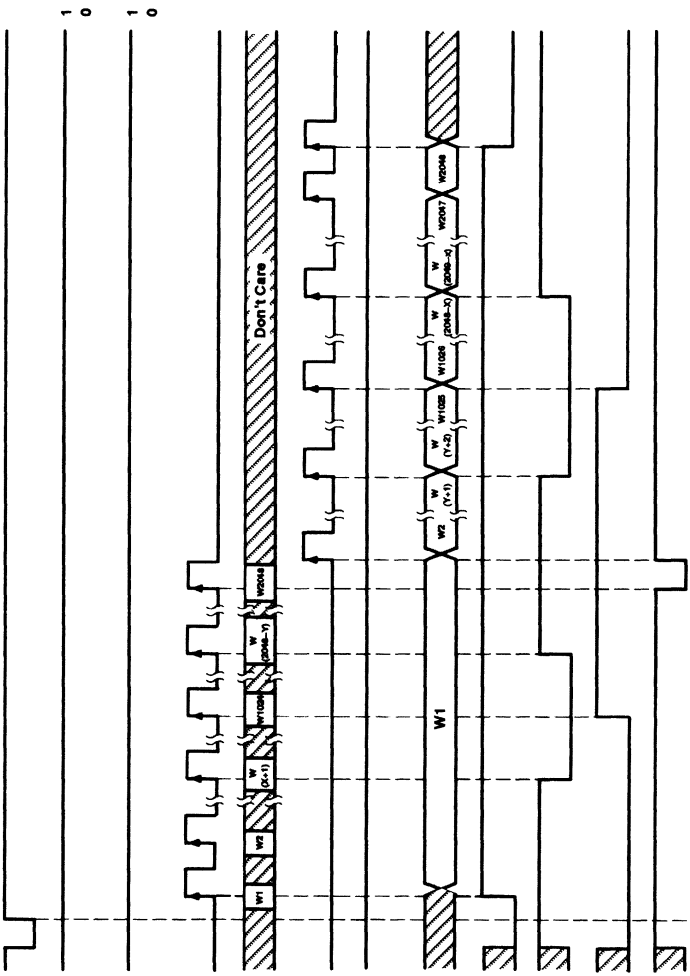



**Figure 1. Timing Diagram to Program X and Y Separately**

## timing diagram



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | 'ACT7808-20 | | 'ACT7808-25 | | 'ACT7808-30 | | 'ACT7808-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | XI | 3.85 | | 3.85 | | 3.85 | | 3.85 | | V |
| | | Other inputs | 2 | | 2 | | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −8 | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 50 | | 40 | | 33.3 | | 25 | MHz |
| $t_w$ | Pulse duration | LDCK high or low | 8 | | 9 | | 11 | | 13 | | ns |
| | | UNCK high or low | 8 | | 9 | | 11 | | 13 | | |
| | | $\overline{PEN}$ low | 9 | | 9 | | 16 | | 13 | | |
| | | $\overline{RESET}$ low | 10 | | 13 | | 16 | | 19 | | |
| $t_{su}$ | Setup time | Data in (D0–D8, DP9) before LDCK↑ | 5 | | 5 | | 5 | | 5 | | ns |
| | | LDCK inactive before $\overline{RESET}$ high | 5 | | 5 | | 5 | | 5 | | |
| | | $\overline{PEN}$ before LDCK↑ | 5 | | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time | Data in (D0–D8, DP9) after LDCK↑ | 0 | | 0 | | 0 | | 0 | | ns |
| | | LDCK inactive after $\overline{RESET}$ high | 5 | | 5 | | 5 | | 5 | | |
| | | $\overline{PEN}$ low after LDCK↑ | 4 | | 4 | | 4 | | 4 | | |
| | | $\overline{PEN}$ high after LDCK low | 0 | | 0 | | 0 | | 0 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | 400 | μA |
| $\Delta I_{CC}$‡ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 6 and 7)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7808-20 | | | 'ACT7808-25 | | 'ACT7808-30 | | 'ACT7808-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK or UNCK | | 50 | | | 40 | | 33.3 | | 25 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | 5 | | 20 | 5 | 22 | 5 | 25 | 5 | 28 | ns |
| $t_{pd}$ | UNCK↑ | | 4.5 | 11 | 15 | 4.5 | 18 | 4.5 | 20 | 4.5 | 22 | |
| $t_{pd}$§ | | | | 10 | | | | | | | | |
| $t_{PLH}$ | LDCK↑ | EMPTY | 4 | | 15 | 4 | 17 | 4 | 19 | 4 | 21 | ns |
| $t_{PHL}$ | UNCK↑ | | 2 | | 15 | 2 | 17 | 2 | 19 | 2 | 21 | |
| $t_{PHL}$ | RESET low | | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | |
| $t_{PHL}$ | LDCK↑ | FULL | 4 | | 15 | 4 | 17 | 4 | 19 | 4 | 21 | ns |
| $t_{PLH}$ | UNCK↑ | | 4 | | 14 | 4 | 16 | 4 | 18 | 4 | 20 | |
| $t_{PLH}$ | RESET low | | 2 | | 18 | 2 | 20 | 2 | 22 | 2 | 24 | |
| $t_{pd}$ | LDCK↑ | AF/AE | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| $t_{pd}$ | UNCK↑ | | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | |
| $t_{PLH}$ | RESET low | | 0 | | 10 | 0 | 12 | 0 | 14 | 0 | 16 | |
| $t_{PLH}$ | LDCK↑ | HF | 2 | | 19 | 2 | 21 | 2 | 23 | 2 | 25 | ns |
| $t_{PHL}$ | UNCK↑ | | 2 | | 16 | 2 | 18 | 2 | 20 | 2 | 22 | |
| $t_{PHL}$ | RESET low | | 2 | | 12 | 2 | 14 | 2 | 16 | 2 | 18 | |
| $t_{PLH}$ | UNCK↑ | XO | 2 | | 11 | 2 | 13 | 2 | 15 | 2 | 17 | ns |
| $t_{PHL}$ | LDCK↑ | | 2 | | 11 | 2 | 13 | 2 | 15 | 2 | 17 | |
| $t_{en}$ | OE | Any Q | 1 | | 10 | 1 | 12 | 1 | 14 | 1 | 16 | ns |
| $t_{dis}$ | | | 1 | | 9 | 1 | 11 | 1 | 13 | 1 | 15 | |
| $t_{en}$ | XI high | Any Q | 3 | | 13 | 3 | 15 | 3 | 17 | 3 | 19 | ns |
| $t_{dis}$ | XO high | | | | 4 | | 4 | | 4 | | 4 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ This is the increase in supply current for each input, excluding XI, that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

§ This parameter is measured with $C_L$ = 30 pF (see Figure 4).

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per FIFO channel | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | 91 | pF |

## APPLICATION INFORMATION

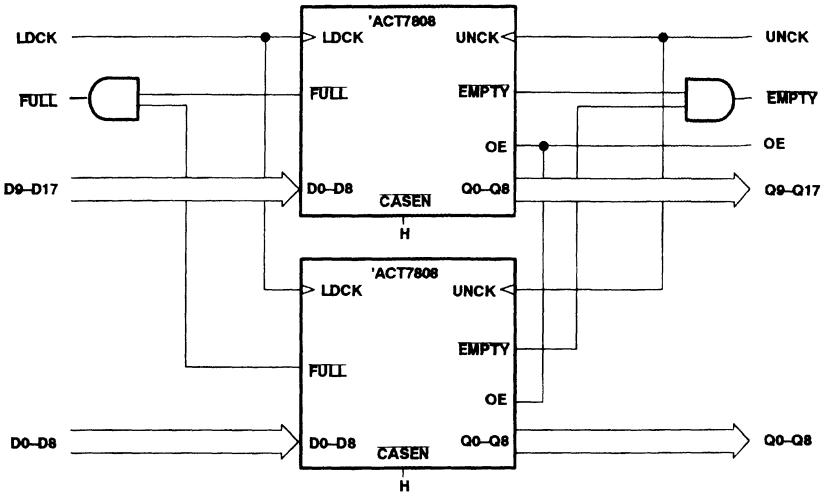



**Figure 2. Word-Width Expansion: 2048 Words by 18 Bits**

### depth cascading

The SN74ACT7808 provides expansion logic necessary for cascading an unlimited number of the FIFOs in depth. $\overline{\text{CASEN}}$ must be low on all FIFOs used in depth expansion. $\overline{\text{FL}}$ must be tied low on the first FIFO in the chain; all others must have $\overline{\text{FL}}$ tied high. The expansion out (XO) output of a FIFO must be tied to the expansion in (XI) input of the next FIFO in the chain. The XO output of the last FIFO is tied to the XI input of the first FIFO to complete the loop. Data buses are common to each FIFO in the chain. A composite $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ signal must be generated to indicate boundary conditions.

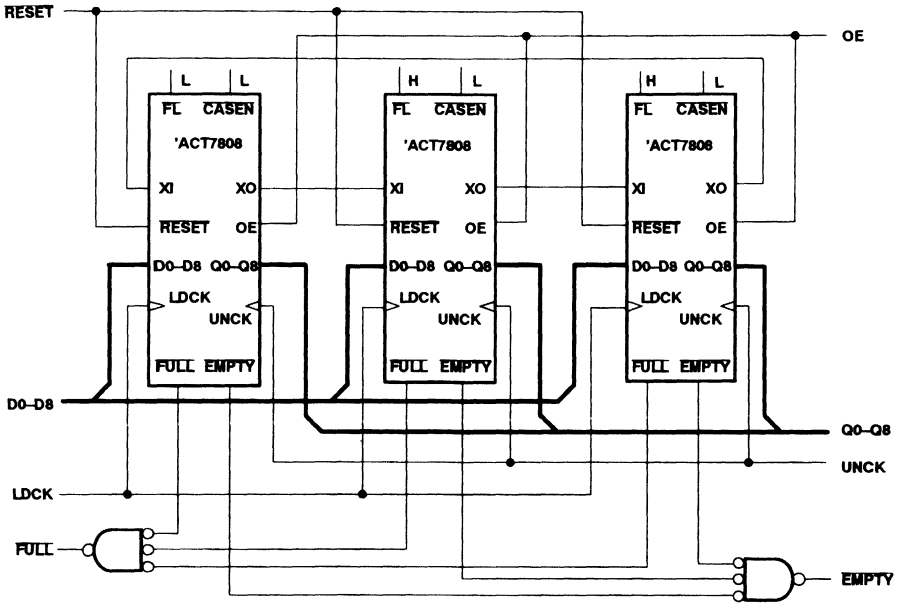



**Figure 3. Depth Cascading to Form a 6K × 9 FIFO**

## TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

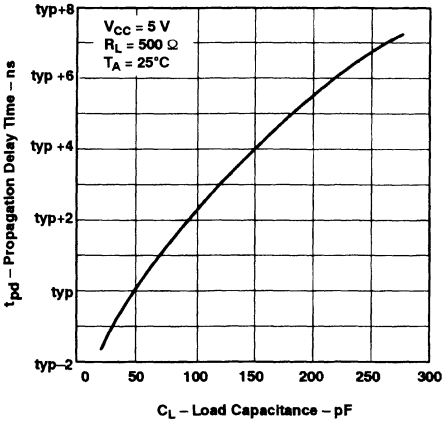



Figure 4

SUPPLY CURRENT
vs
CLOCK FREQUENCY

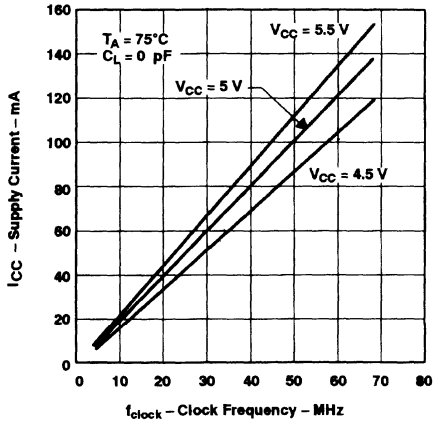



Figure 5

### calculating power dissipation

With $I_{CCF}$ taken from Figure 5, the maximum power dissipation may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

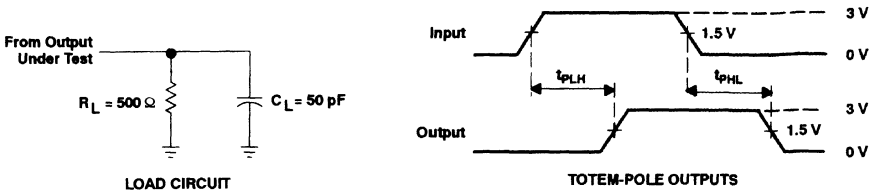
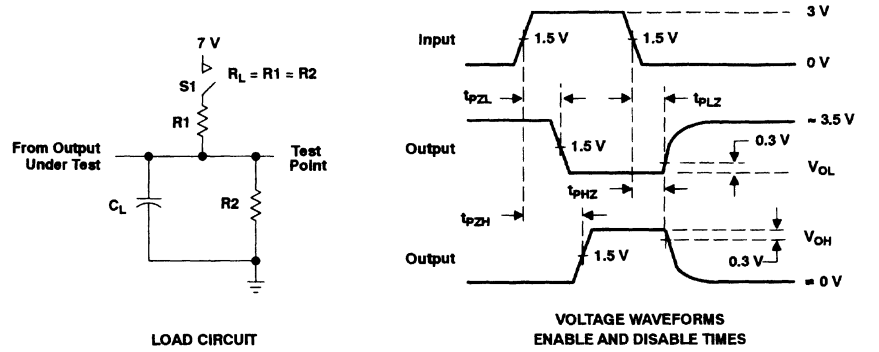



**Figure 6. Standard CMOS Outputs (XO, EMPTY, FULL, AF/AE, HF)**




| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{wl}$ | | 500 Ω | 50 pF | Open |

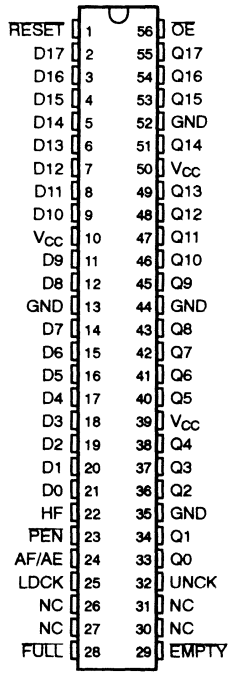
† Includes probe and test fixture capacitance.

**Figure 7. 3-State Outputs (Any Q)**

SCAS209–D4023, SEPTEMBER 1991–REVISED APRIL 1992

- **Member of the Texas Instruments *Widebus* ™ Family**
- **Load Clock and Unload Clock May Be Asynchronous or Coincident**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**
- **64 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost Full/Almost Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7804 and SN74ACT7806**

DL PACKAGE
(TOP VIEW)




## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7814 is a 64-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 64. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost full/almost empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full and high when the memory is not full. The $\overline{EMPTY}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 32 or more words and is low when it contains 31 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{PEN}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (64 minus Y) or more words. The AF/AE flag is low when the FIFO contains between (X plus 1) and (63 minus Y) words.

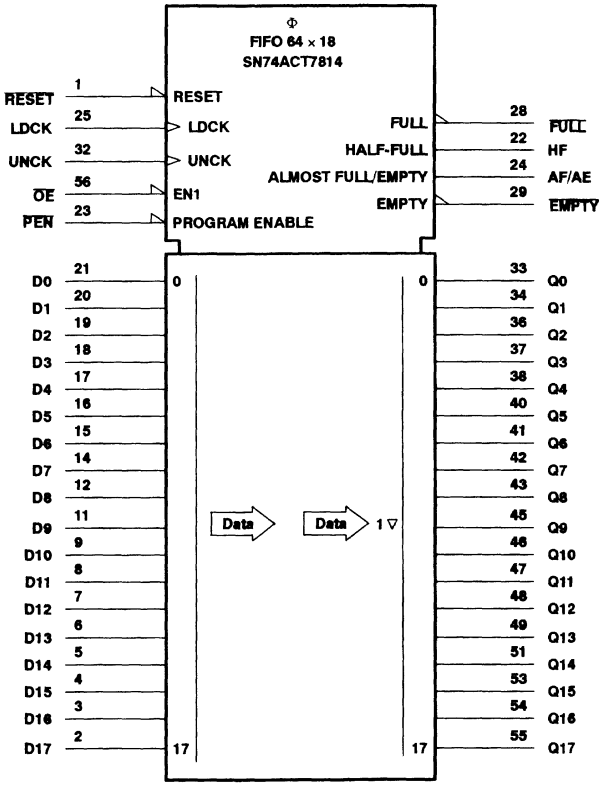
A low level on the reset ($\overline{RESET}$) input resets the internal stack pointers and sets $\overline{FULL}$ high, HF low, and $\overline{EMPTY}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

Widebus is a trademark of Texas Instruments Incorporated.

## description (continued)

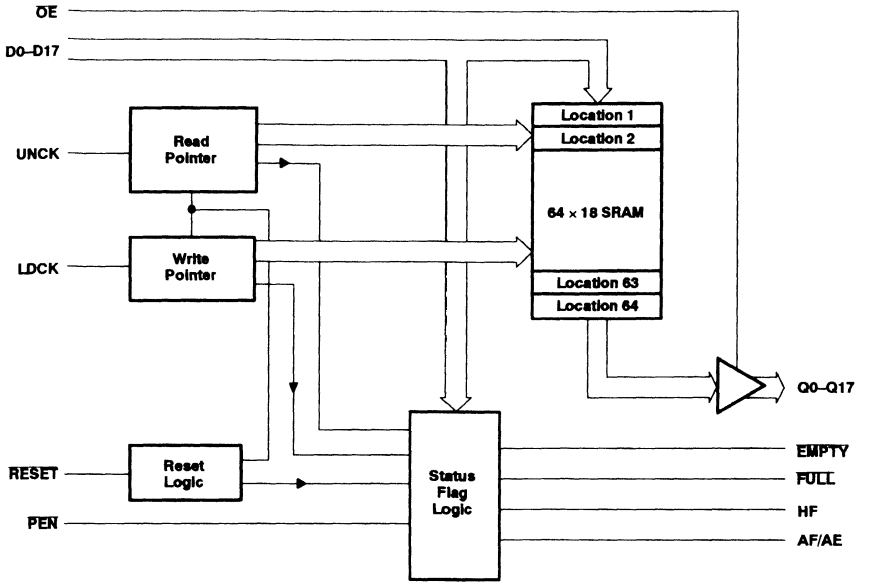
The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is high.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## functional block diagram



## Terminal Functions

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AF/AE | 24 | O | Almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 8 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (64 minus Y) or more words. AF/AE is high after reset. |
| D0–D17 | 21–14, 12–11, 9–2 | I | 18-bit data input port |
| $\overline{\text{EMPTY}}$ | 29 | O | Empty flag. $\overline{\text{EMPTY}}$ is high when the FIFO memory is not empty; $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty or upon assertion of $\overline{\text{RESET}}$. |
| $\overline{\text{FULL}}$ | 28 | O | Full flag. $\overline{\text{FULL}}$ is high when the FIFO memory is not full or upon assertion of $\overline{\text{RESET}}$; $\overline{\text{FULL}}$ is low when the FIFO memory is full. |
| HF | 22 | O | Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset. |
| LDCK | 25 | I | Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high. |
| $\overline{\text{OE}}$ | 56 | I | Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state. |
| $\overline{\text{PEN}}$ | 23 | I | Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high. |
| Q0–Q17 | 33–34, 36–38, 40–43, 45–49, 51, 53–55 | O | 18-bit data output port |
| $\overline{\text{RESET}}$ | 1 | I | Reset. A low level on this input resets the FIFO and drives $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low. |
| UNCK | 32 | I | Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high. |

### offset values for AF/AE

The almost full/almost empty flag has two programmable limits, the almost empty offset value (X) and the almost full offset value (Y). They may be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag will be high when the FIFO contains X or less words or (64 minus Y) or more words.

To program the offset values, $\overline{PEN}$ may be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D4 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of LDCK will reprogram Y to the binary value on D0–D4 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed.

A maximum value of 31 may be programmed for either X or Y. To use the default values of X = Y = 8, $\overline{PEN}$ must be held high.

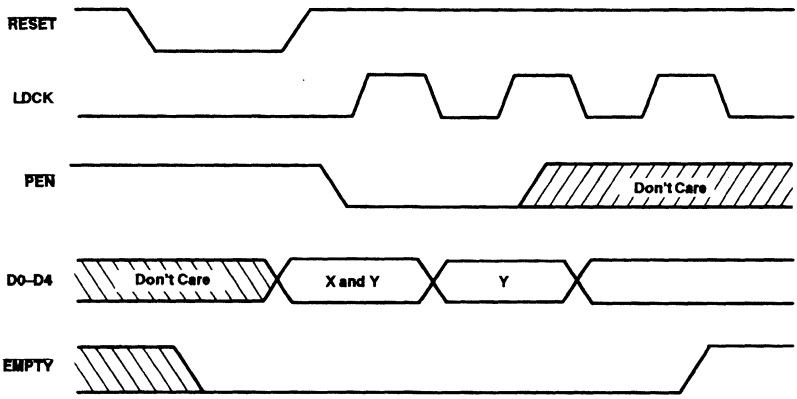
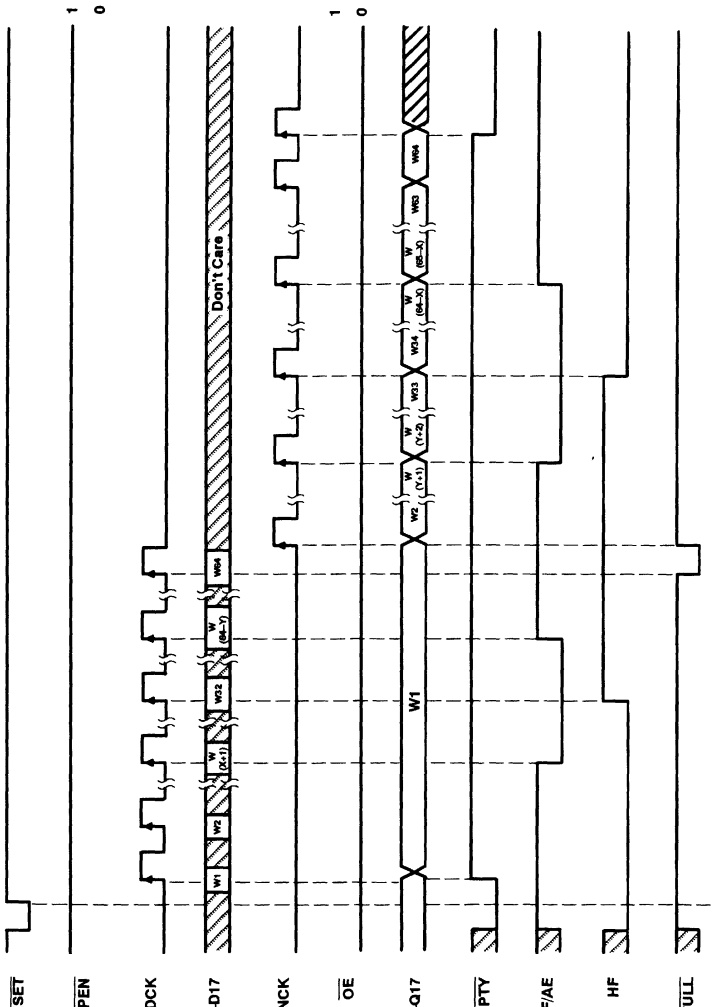



**Figure 1. Programming X and Y Separately**

## timing diagram






TEXAS INSTRUMENTS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | 'ACT7814-20 | | 'ACT7814-25 | | 'ACT7814-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | | −8 | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | | 16 | | 16 | mA |
| | | Flags | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | | | 50 | | 40 | | 25 | MHz |
| $t_w$ | Pulse duration | LDCK high or low | 7 | | 8 | | 12 | | ns |
| | | UNCK high or low | 7 | | 8 | | 12 | | |
| | | $\overline{PEN}$ low | 7 | | 8 | | 12 | | |
| | | $\overline{RESET}$ low | 10 | | 10 | | 12 | | |
| $t_{su}$ | Setup time | Data in (D0–D17) before LDCK↑ | 5 | | 5 | | 5 | | ns |
| | | $\overline{PEN}$ before LDCK↑ | 5 | | 5 | | 5 | | |
| | | LDCK inactive before $\overline{RESET}$ high | 5 | | 6 | | 6 | | |
| $t_h$ | Hold time | Data in (D0–D17) after LDCK↑ | 0 | | 0 | | 0 | | ns |
| | | LDCK inactive after $\overline{RESET}$ high | 5 | | 6 | | 6 | | |
| | | $\overline{PEN}$ low after LDCK↑ | 3 | | 3 | | 3 | | |
| | | $\overline{PEN}$ high after LDCK↓ | 0 | | 0 | | 0 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 5 and 6)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7814-20 | | | 'ACT7814-25 | | 'ACT7814-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK or UNCK | | 50 | | | 40 | | 25 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | 9 | | 20 | 9 | 22 | 9 | 24 | ns |
| $t_{pd}$ | UNCK↑ | | 6 | 11.5 | 15 | 6 | 18 | 6 | 20 | |
| $t_{pd}$‡ | UNCK↑ | | | 10.5 | | | | | | |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | 6 | | 15 | 6 | 17 | 6 | 19 | ns |
| $t_{PHL}$ | UNCK↑ | | 6 | | 15 | 6 | 17 | 6 | 19 | |
| $t_{PHL}$ | $\overline{RESET}$ low | | 4 | | 16 | 4 | 18 | 4 | 20 | |
| $t_{PHL}$ | LDCK↑ | $\overline{FULL}$ | 6 | | 15 | 6 | 17 | 6 | 19 | ns |
| $t_{PLH}$ | UNCK↑ | | 6 | | 15 | 6 | 17 | 6 | 19 | |
| $t_{PLH}$ | $\overline{RESET}$ low | | 4 | | 18 | 4 | 20 | 4 | 22 | |
| $t_{pd}$ | LDCK↑ | AF/AE | 7 | | 18 | 7 | 20 | 7 | 22 | ns |
| $t_{pd}$ | UNCK↑ | | 7 | | 18 | 7 | 20 | 7 | 22 | |
| $t_{PLH}$ | $\overline{RESET}$ low | | 2 | | 10 | 2 | 12 | 2 | 14 | |
| $t_{PLH}$ | LDCK↑ | HF | 5 | | 18 | 5 | 20 | 5 | 22 | ns |
| $t_{PHL}$ | UNCK↑ | | 7 | | 18 | 7 | 20 | 7 | 22 | |
| $t_{PHL}$ | $\overline{RESET}$ low | | 3 | | 12 | 3 | 14 | 3 | 16 | |
| $t_{en}$ | $\overline{OE}$ | Any Q | 2 | | 9 | 2 | 10 | 2 | 11 | ns |
| $t_{dis}$ | | | 2 | | 10 | 2 | 11 | 2 | 12 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This parameter is measured at $C_L$ = 30 pF (see Figure 3).

**operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per FIFO channel | Outputs enabled | $C_L$ = 50 pF, f = 5 MHz | 53 | pF |

## APPLICATION INFORMATION

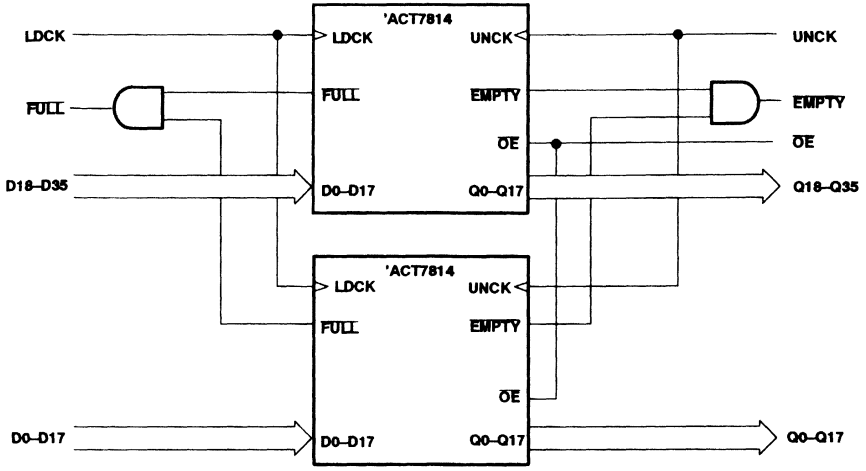



**Figure 2. Word-Width Expansion: 64 Words by 36 Bits**

## TYPICAL CHARACTERISTICS

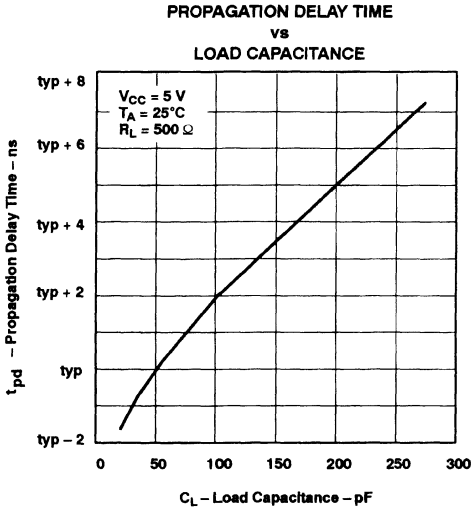



Figure 3

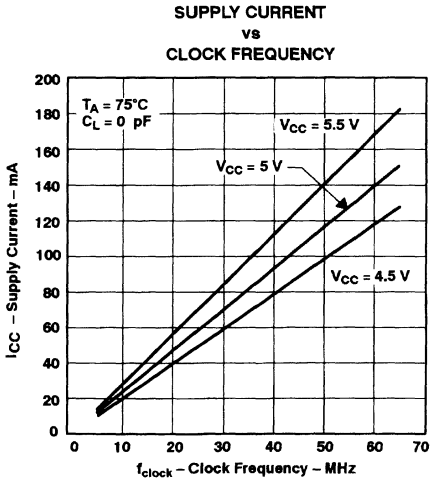



Figure 4

### calculating power dissipation

With $I_{CCF}$ taken from Figure 4, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION

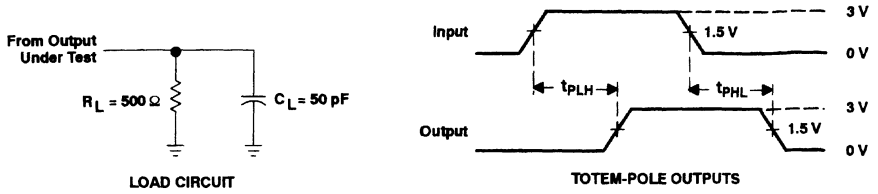
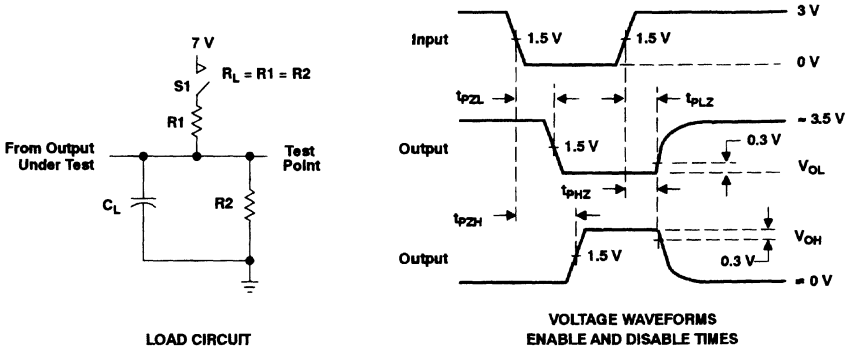



Figure 5. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)




| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

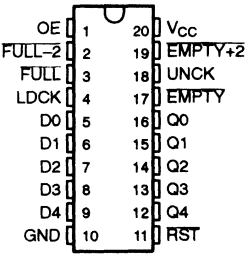
† Includes probe and test fixture capacitance.

Figure 6. 3-State Outputs (Any Q)

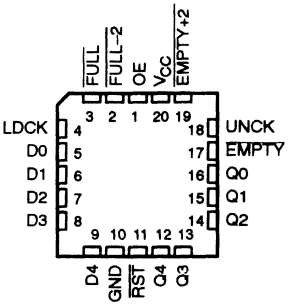
D3486, MARCH 1990–REVISED JUNE 1992

- **Independent Asynchronous Inputs and Outputs**
- **16 Words by 5 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)




FN PACKAGE
(TOP VIEW)




## description

This 80-bit memory uses Advanced Low-Power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

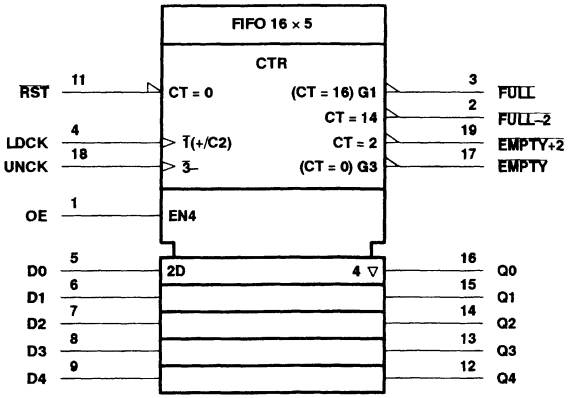
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{FULL+2}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–2}}$ output is low when the memory contains 14 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+2}}$ output is low when two words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{EMPTY+2}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK after either a $\overline{\text{RST}}$ pulse or from an empty condition causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS229B is characterized for operation from 0°C to 70°C.

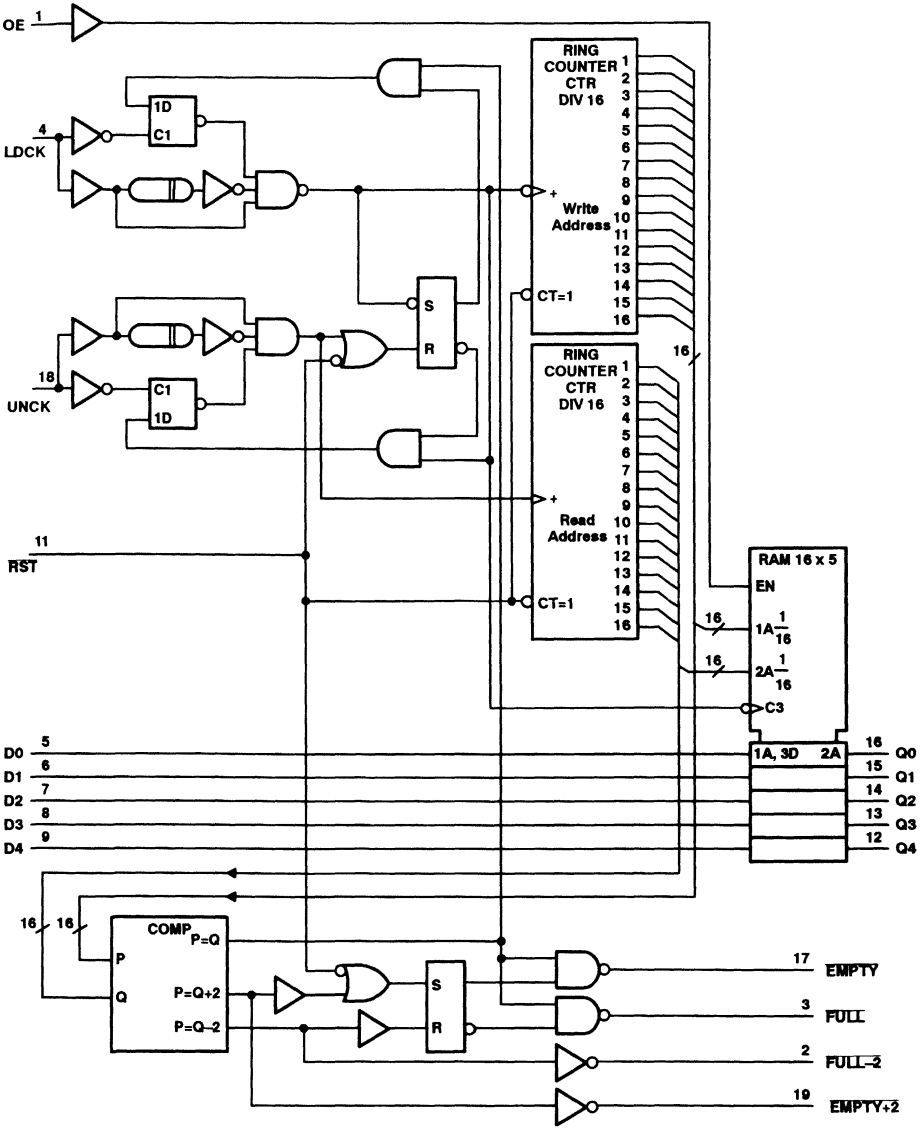
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

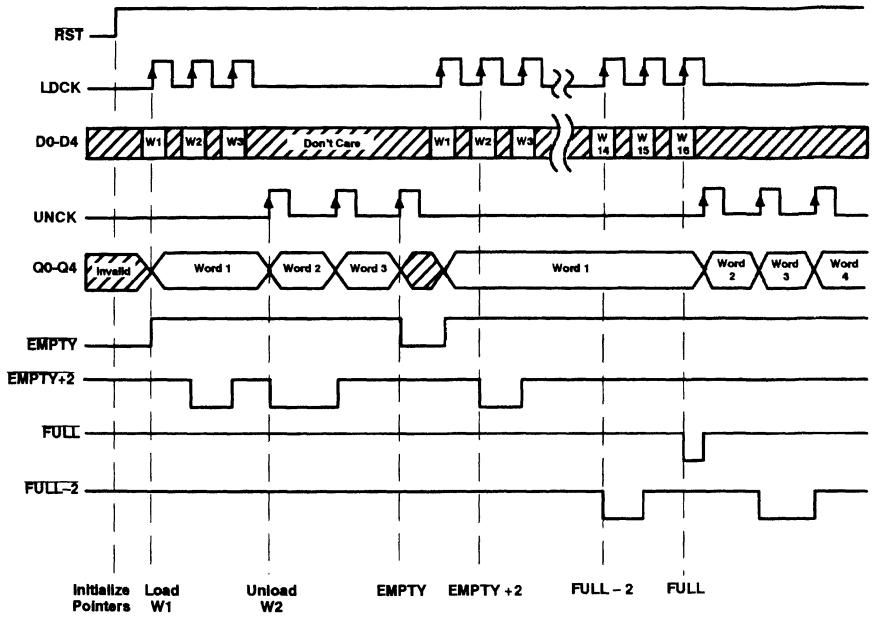
Pin numbers shown are for DW and N packages.

## logic diagram (positive logic)




Pin numbers shown are for DW and N packages.

## timing diagram




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ ..... 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs | | | −1.6 | mA |
| | | Status flags | | | −0.4 | |
| $I_{OL}$ | Low-level output current | Q outputs | | | 24 | mA |
| | | Status flags | | | 8 | |
| $f_{clock}$ | Clock frequency | LDCK | 0 | | 40 | MHz |
| | | UNCK | 0 | | 40 | |
| $t_w$ | Pulse duration | $\overline{RST}$ low | 18 | | | ns |
| | | LDCK low | 15 | | | |
| | | LDCK high | 10 | | | |
| | | UNCK low | 15 | | | |
| | | UNCK high | 10 | | | |
| $t_{su}$ | Setup time | Data before LDCK↑ | 8 | | | ns |
| | | $\overline{RST}$ (inactive) before LDCK↑ | 5 | | | |
| | | LDCK (inactive) before $\overline{RST}$↑ | 5 | | | |
| $t_h$ | Hold time | Data after LDCK↑ | 5 | | | ns |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the $V_{IL}$, $V_{IH}$, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = −2.6 mA | 2.4 | 3.2 | | V |
| | Status flags | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OL}$ = −0.4 mA | $V_{CC}$−2 | | | |
| $V_{OL}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | Status flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 85 | 140 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

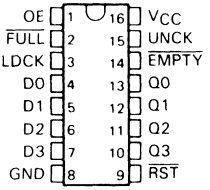
## switching characteristics

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 0°C to 70°C | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | LDCK, UNCK | | 40 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | 6 | 30 | ns |
| | UNCK↑ | | 6 | 30 | |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | 5 | 25 | ns |
| $t_{PHL}$ | UNCK↑ | | 6 | 27 | |
| $t_{PHL}$ | $\overline{RST}$↓ | $\overline{EMPTY}$ | 5 | 26 | ns |
| $t_{pd}$ | LDCK↑ | $\overline{EMPTY+2}$ | 7 | 33 | ns |
| | UNCK↑ | | 9 | 35 | |
| $t_{PLH}$ | $\overline{RST}$↓ | $\overline{EMPTY+2}$ | 9 | 33 | ns |
| $t_{pd}$ | LDCK↑ | $\overline{FULL-2}$ | 7 | 33 | ns |
| | UNCK↑ | | 9 | 35 | |
| $t_{PLH}$ | $\overline{RST}$↓ | $\overline{FULL-2}$ | 9 | 33 | ns |
| $t_{PHL}$ | LDCK↑ | $\overline{FULL}$ | 6 | 27 | ns |
| $t_{PLH}$ | UNCK↑ | $\overline{FULL}$ | 5 | 25 | ns |
| | $\overline{RST}$↓ | | 8 | 31 | |
| $t_{en}$ | OE↑ | Q | 2 | 15 | ns |
| $t_{dis}$ | OE↓ | Q | 1 | 15 | ns |

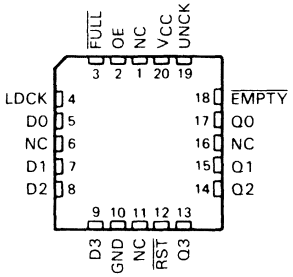
SDIS010A – D3247, FEBRUARY 1989

- **Independent Asynchronous Inputs and Outputs**
- **Package Options Include Plastic Small-Outline Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **16 Words by 4 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Type**
- **3-State Outputs**

**DW OR N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

This 64-bit memory uses Advanced Low-Power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 4 bits each.

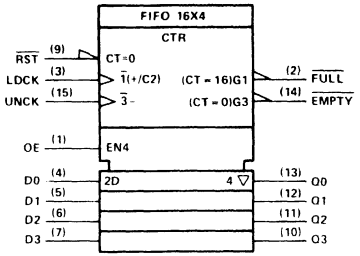
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

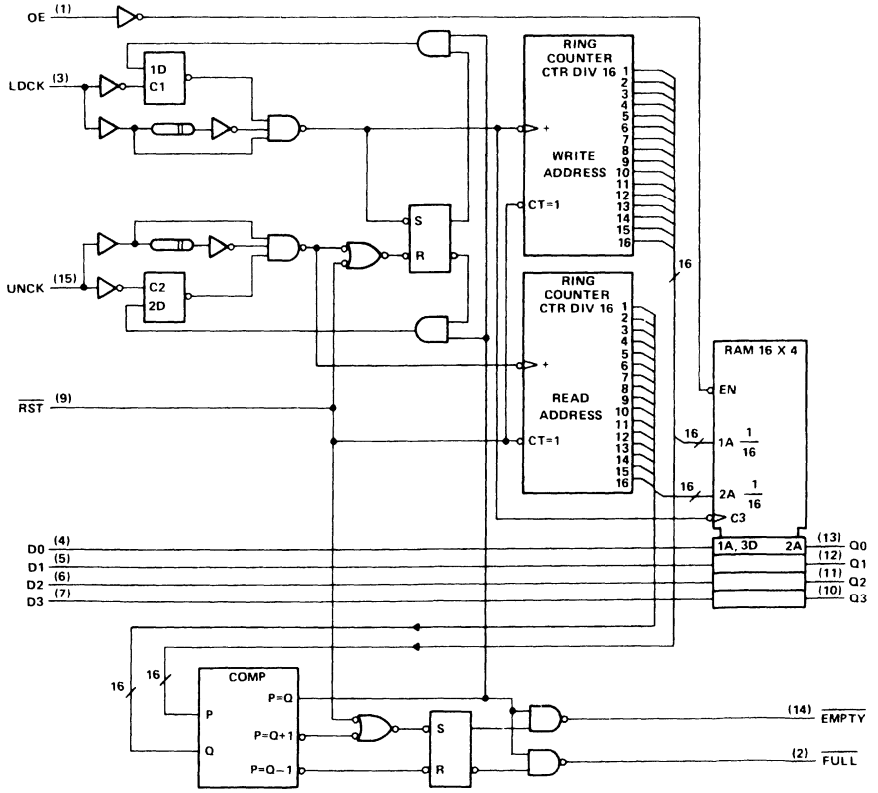
A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

## logic symbol†



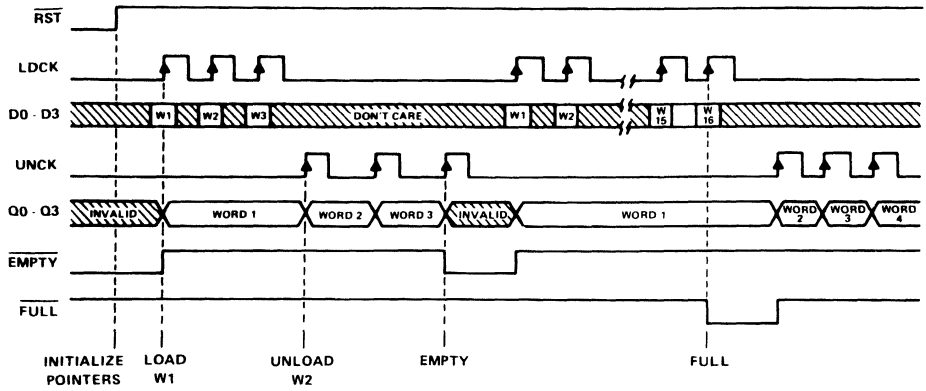

† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

## logic diagram (positive logic)




Pin numbers shown are for DW and N packages.

## timing diagram




## absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

## recommended operating conditions (see Note 1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs | | | −2.6 | mA |
| | | $\overline{FULL}$, $\overline{EMPTY}$ | | | −0.4 | |
| $I_{OL}$ | Low-level output current | Q outputs | | | 24 | mA |
| | | $\overline{FULL}$, $\overline{EMPTY}$ | | | 8 | |
| $f_{clock}$† | Clock frequency | LDCK | 0 | | 40 | MHz |
| | | UNCK | 0 | | 40 | |
| $t_w$ | Pulse duration | $\overline{RST}$ low | 18 | | | ns |
| | | LDCK low | 15 | | | |
| | | LDCK high | 10 | | | |
| | | UNCK low | 15 | | | |
| | | UNCK high | 10 | | | |
| $t_{su}$ | Setup time | Data before LDCK↑ | 8 | | | ns |
| | | LDCK inactive before $\overline{RST}$↑ | 5 | | | |
| $t_h$ | Hold time | Data after LDCK↑ | 5 | | | ns |
| | | LDCK inactive after $\overline{RST}$↑ | 5 | | | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

†The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

NOTE 1: To ensure proper operation, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum $V_{IL}$, minimum $V_{IH}$, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $\overline{FULL}$, EMPTY | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2.6 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | $\overline{FULL}$, $\overline{EMPTY}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = 4 mA | | 0.25 | 0.4 | |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 80 | 125 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

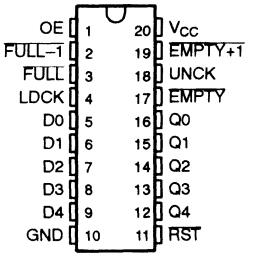
## switching characteristics

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 0°C to 70°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | LDCK | | | 50 | | 40 | | MHz |
| | UNCK | | | 50 | | 40 | | |
| $t_{pd}$ | LDCK↑ | Any Q | | 14 | 23 | 6 | 30 | ns |
| $t_{pd}$ | UNCK↑ | Any Q | | 15 | 23 | 6 | 30 | ns |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | | 13 | 20 | 5 | 25 | ns |
| $t_{PHL}$ | UNCK↑ | $\overline{EMPTY}$ | | 15 | 22 | 6 | 27 | ns |
| $t_{PHL}$ | $\overline{RST}$↓ | $\overline{EMPTY}$ | | 15 | 21 | 5 | 26 | ns |
| $t_{PHL}$ | LDCK↑ | $\overline{FULL}$ | | 15 | 22 | 6 | 27 | ns |
| $t_{PLH}$ | UNCK↑ | $\overline{FULL}$ | | 13 | 20 | 5 | 25 | ns |
| $t_{PLH}$ | $\overline{RST}$↓ | $\overline{FULL}$ | | 16 | 23 | 7 | 28 | ns |
| $t_{en}$ | OE↑ | Q | | 5 | 12 | 1 | 14 | ns |
| $t_{dis}$ | OE↓ | Q | | 5 | 12 | 1 | 16 | ns |

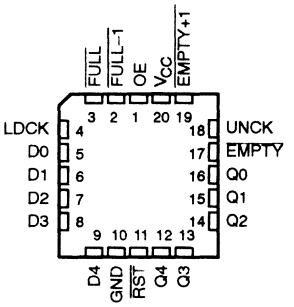
D3487, MARCH 1990–REVISED JUNE 1992

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




## description

This 80-bit memory uses Advanced Low-Power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

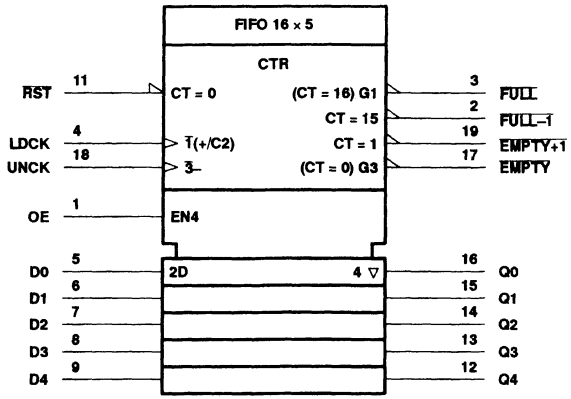
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL}-1}$, and $\overline{\text{FULL}+1}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL}-1}$ output is low when the memory contains 15 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY}+1}$ output is low when two words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL}-1}$, and $\overline{\text{EMPTY}+1}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

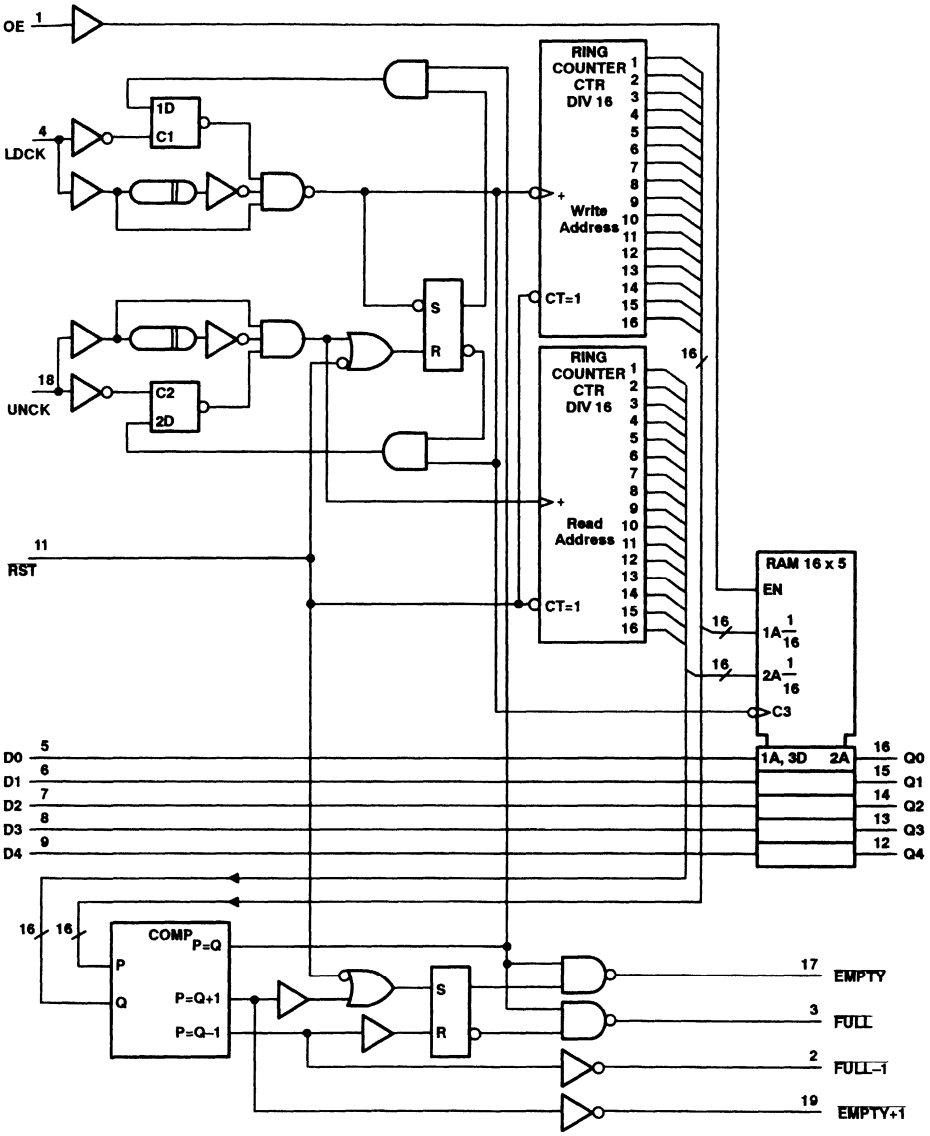
The SN74ALS233B is characterized for operation from 0°C to 70°C.

## logic symbol†



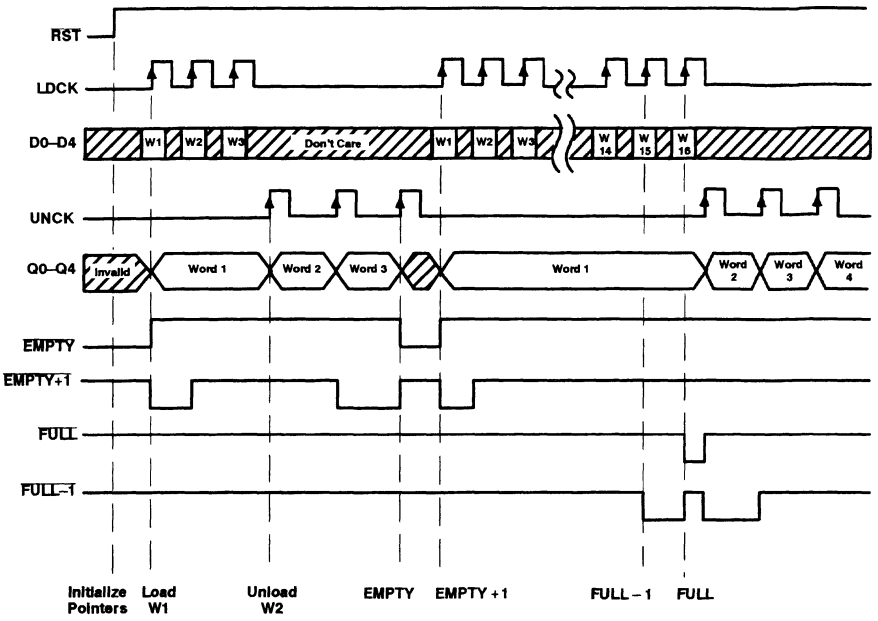

† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.
Pin numbers shown are for DW and N packages.

## logic diagram (positive logic)




Pin numbers shown are for DW and N packages.

## timing diagram




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ ..... 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs | | | −1.6 | mA |
| | | Status flags | | | −0.4 | |
| $I_{OL}$ | Low-level output current | Q outputs | | | 24 | mA |
| | | Status flags | | | 8 | |
| $f_{clock}$ | Clock frequency | LDCK | 0 | | 40 | MHz |
| | | UNCK | 0 | | 40 | |
| $t_w$ | Pulse duration | $\overline{RST}$ low | 18 | | | ns |
| | | LDCK low | 15 | | | |
| | | LDCK high | 10 | | | |
| | | UNCK low | 15 | | | |
| | | UNCK high | 10 | | | |
| $t_{su}$ | Setup time | Data before LDCK↑ | 8 | | | ns |
| | | $\overline{RST}$ (inactive) before LDCK↑ | 5 | | | |
| | | LDCK (inactive) before $\overline{RST}$↑ | 5 | | | |
| $t_h$ | Hold time | Data after LDCK↑ | 5 | | | ns |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the $V_{IL}$, $V_{IH}$, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2.6 mA | 2.4 | 3.2 | | V |
| | Status flags | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | |
| $V_{OL}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | Status flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 88 | 133 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

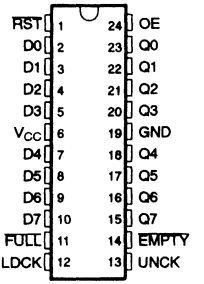
## switching characteristics

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 0°C to 70°C | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | LDCK, UNCK | | 40 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | 6 | 32 | ns |
| | UNCK↑ | | 6 | 30 | |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | 5 | 25 | ns |
| $t_{PHL}$ | UNCK↑ | | 6 | 27 | |
| $t_{PHL}$ | $\overline{RST}$↓ | $\overline{EMPTY}$ | 5 | 25 | ns |
| $t_{pd}$ | LDCK↑ | $\overline{EMPTY+1}$ | 7 | 34 | ns |
| | UNCK↑ | | 7 | 34 | |
| $t_{PLH}$ | $\overline{RST}$↓ | $\overline{EMPTY+1}$ | 8 | 31 | ns |
| $t_{pd}$ | LDCK↑ | $\overline{FULL-1}$ | 9 | 33 | ns |
| | UNCK↑ | | 8 | 32 | |
| $t_{PLH}$ | $\overline{RST}$↓ | $\overline{FULL-1}$ | 11 | 32 | ns |
| $t_{PHL}$ | LDCK↑ | $\overline{FULL}$ | 6 | 27 | ns |
| $t_{PLH}$ | UNCK↑ | $\overline{FULL}$ | 5 | 25 | ns |
| | $\overline{RST}$↓ | | 9 | 30 | |
| $t_{en}$ | OE↑ | Q | 2 | 15 | ns |
| $t_{dis}$ | OE↓ | Q | 1 | 15 | ns |

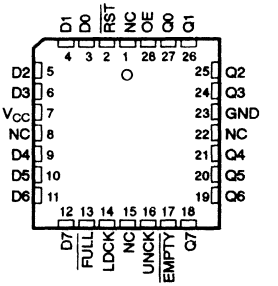
D3091, FEBRUARY 1988–REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 8 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

**NT PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




NC–No internal connection

## description

This 512-bit memory uses Advanced Low-Power Schottky IMPACT-X ™ technology and features high speed and fast fall-through times. It is organized as 64 words by 8 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock (LDCK) input and is read out on a low-to-high transition of the unload clock (UNCK) input. The memory is full when the number of words clocked in exceed by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the the memory is empty, UNCK signals have no effect.

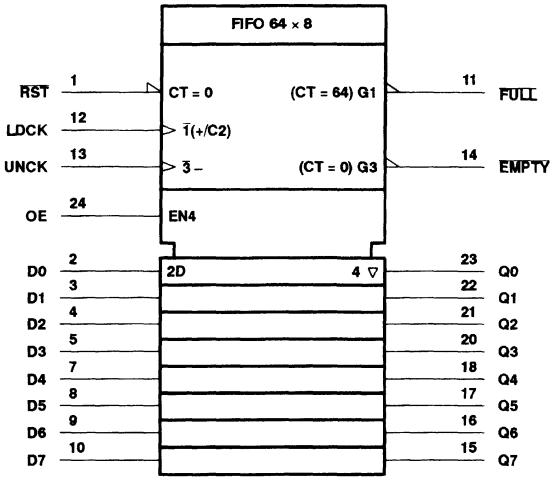
Status of the FIFO memory is monitored by the FULL and EMPTY output flags. The FULL output will be low when the memory is full, and high when the memory is not full. The EMPTY output will be low when the memory is empty, and high when it is not empty.

A low level on the reset (RST) input resets the internal stack control pointers and also sets EMPTY low and FULL high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a RST pulse or from an empty condition, causes EMPTY to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable (OE) input is low. The OE input does not effect either the FULL or EMPTY output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2232A is characterized for operation from 0°C to 70°C.

IMPACT-X is a trademark of Texas Instruments Incorporated.

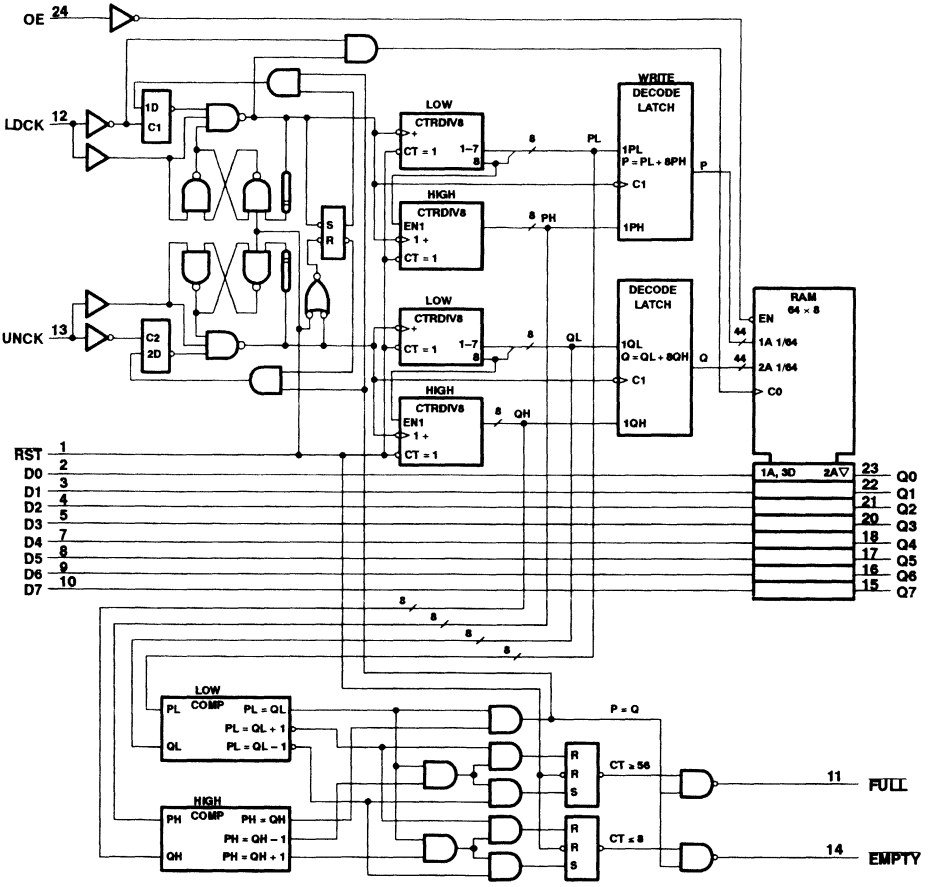
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

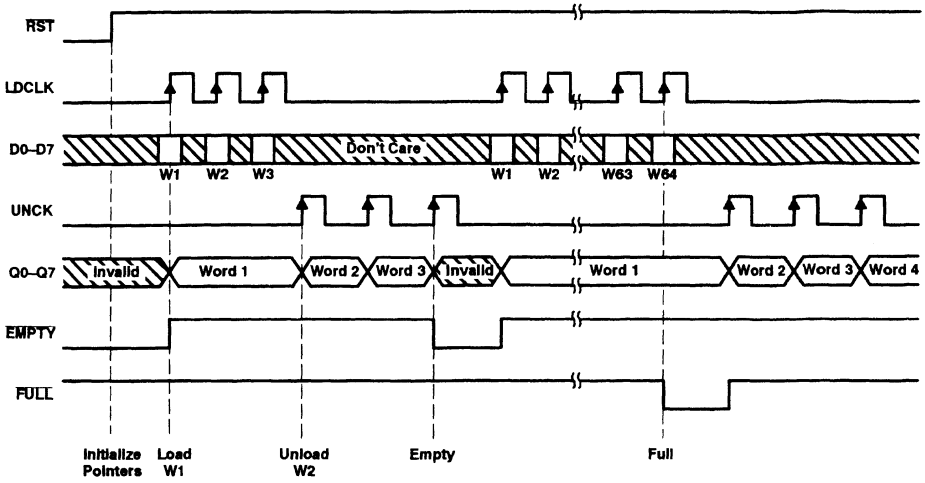
Pin numbers shown are for the NT package.

## logic diagram (positive logic)




Pin numbers shown are for the NT package.

## timing diagram




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs | | | −2.6 | mA |
| | | $\overline{FULL}$, $\overline{EMPTY}$ | | | −0.4 | |
| $I_{OL}$ | Low-level output current | Q outputs | | | 24 | mA |
| | | $\overline{FULL}$, $\overline{EMPTY}$ | | | 8 | |
| $f_{clock}$ | Clock frequency | LDCK, UNCK | 0 | | 40 | MHz |
| $t_w$ | Pulse duration | $\overline{RST}$ low | 25 | | | ns |
| | | LDCK low | 13 | | | |
| | | LDCK high | 12 | | | |
| | | UNCK low | 13 | | | |
| | | UNCK high | 12 | | | |
| $t_{su1}$ | Setup time, data before LDCK↑ | | 5 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RST}$ high (inactive) before LDCK↑ | | 5 | | | ns |
| $t_h$ | Hold time, data after LDCK↑ | | 5 | | | ns |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2.6 mA | 2.4 | 3.2 | | V |
| | $\overline{FULL}$, $\overline{EMPTY}$ | $V_{CC}$ = MIN to MAX, | $I_{OH}$ = 0.4 mA | $V_{CC}$−2 | | | |
| $V_{OL}$ | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | $\overline{FULL}$, $\overline{EMPTY}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | CLKS | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| | Others | | | | | −0.1 | |
| $I_O$‡ | Q outputs | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −20 | | −130 | mA |
| | $\overline{FULL}$, $\overline{EMPTY}$ | | | −20 | | −112 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 175 | 270 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

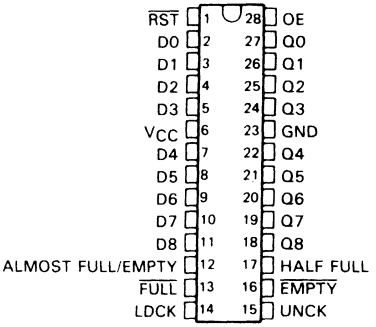
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 0°C to 70°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | LDCK, UNCK | | 40 | | | 40 | | MHz |
| $t_{pd}$ | LDCK↑ | Any Q | | 18 | 26 | | 30 | ns |
| | UNCK↑ | | | 18 | 24 | | 27 | |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | | 12 | 16 | | 18 | ns |
| $t_{PHL}$ | UNCK↑ | | | 12 | 17 | | 20 | |
| $t_{PHL}$ | $\overline{RST}$↓ | $\overline{EMPTY}$ | | 12 | 17 | | 20 | ns |
| $t_{PHL}$ | LDCK↑ | $\overline{FULL}$ | | 16 | 21 | | 22 | ns |
| $t_{PLH}$ | UNCK↑ | $\overline{FULL}$ | | 10 | 15 | | 18 | ns |
| | $\overline{RST}$↓ | | | 13 | 19 | | 23 | |
| $t_{en}$ | OE↑ | Q | | 11 | 15 | | 17 | ns |
| $t_{dis}$ | OE↓ | Q | | 11 | 17 | | 19 | ns |

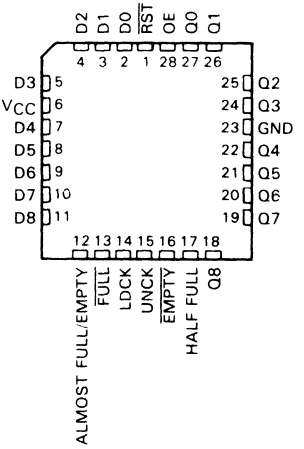
D3092, FEBRUARY 1988—REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words By 9 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

N PACKAGE
(TOP VIEW)




FN PACKAGE
(TOP VIEW)




## description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT—X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 9 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, ALMOST FULL/EMPTY, and HALF FULL output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty and high when it is not empty. The ALMOST FULL/EMPTY flag is high when the FIFO contains eight or less words or fifty-six or more words. The ALMOST FULL/EMPTY flag is low when the FIFO contains between nine and fifty-five words. The HALF FULL flag is high when the FIFO contains thirty-two or more words, and is low when the FIFO contains thirty-one words or less.

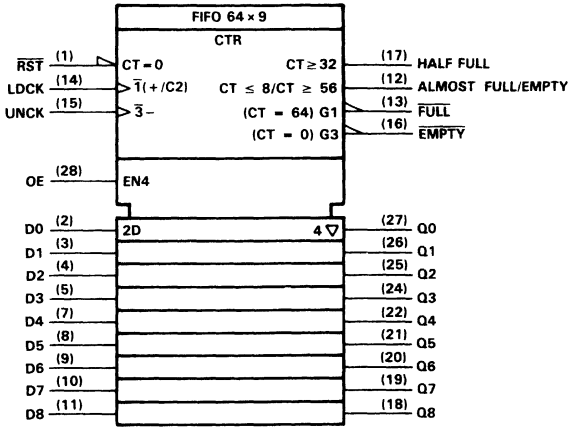
IMPACT—X is a trademark of Texas Instruments Incorporated.

## description (continued)

A low level on the reset input ($\overline{RST}$) resets the internal stack control pointers and also sets EMPTY low and $\overline{FULL}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{RST}$ pulse or from an empty condition, causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not affect either the $\overline{FULL}$ or $\overline{EMPTY}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2233A is characterized for operation from 0°C to 70°C.

## logic symbol†

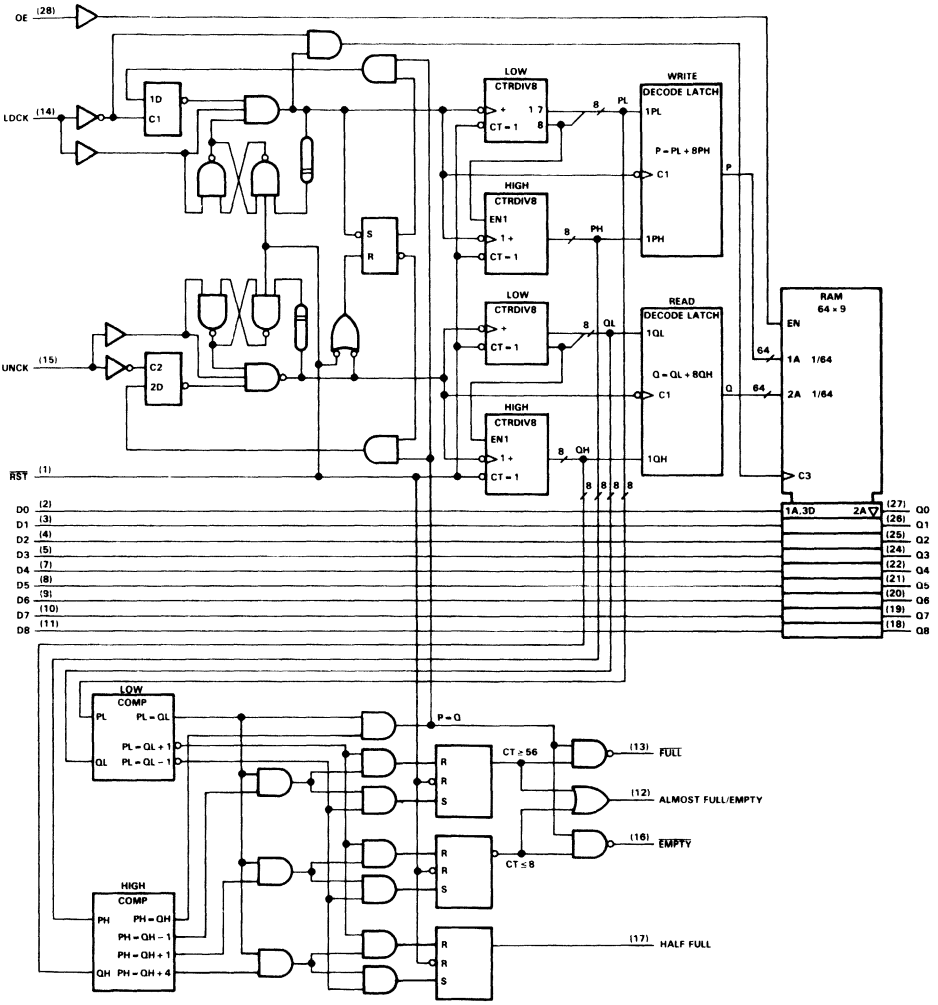



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

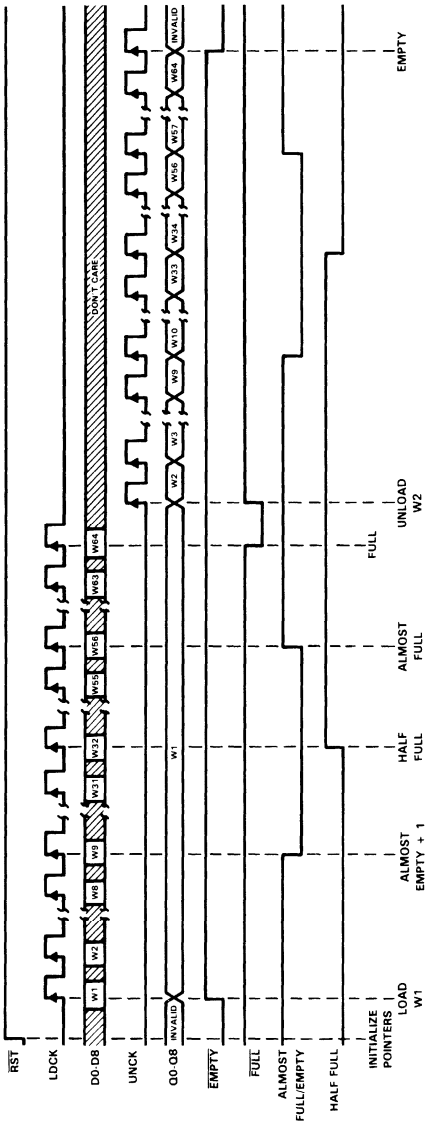
Pin numbers shown are for the N package.

D3092, FEBRUARY 1988 – REVISED MARCH 1990

## logic diagram (positive logic)



## timing diagram






TEXAS INSTRUMENTS

### absolute maximum ratings over operating free-air temperature range

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs | | | −2.6 | mA |
| | | Flag outputs | | | −0.4 | |
| $I_{OL}$ | Low-level output current | Q outputs | | | 24 | mA |
| | | Flag outputs | | | 8 | |
| $f_{clock}$ | Clock frequency | LDCK, UNCK | 0 | | 40 | MHz |
| $t_w$ | Pusle duration | $\overline{RST}$ low | 25 | | | ns |
| | | LDCK low | 13 | | | |
| | | LDCK high | 12 | | | |
| | | UNCK low | 13 | | | |
| | | UNCK high | 12 | | | |
| $t_{su1}$ | Setup time, data before LDCK↑ | | 5 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RST}$ high (inactive) before LDCK↑ | | 5 | | | ns |
| $t_h$ | Hold time, data after LDCK↑ | | 5 | | | ns |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDTIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | 1.2 | V |
| $V_{OH}$ | Flag outputs | $V_{CC}$ = MIN TO MAX, | $I_{OH}$ = 0.4 mA | $V_{CC}$ 2 | | | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2.6 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Q Outputs | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | Flag outputs | | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | |
| | | | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | CLKs | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| | Others | | | | | −0.1 | |
| $I_O$‡ | Q outputs | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −20 | | −130 | mA |
| | Flag outputs | | | −20 | | −112 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 175 | 290 | mA |

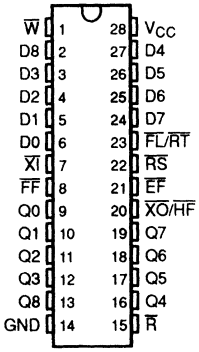
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics

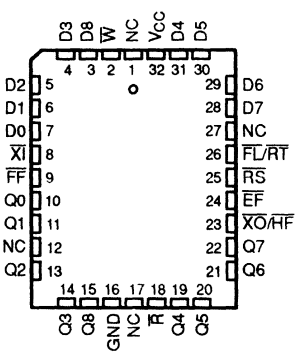
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 0°C to 70°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | LDCK | | | | | 40 | | MHz |
| | UNCK | | | | | 40 | | |
| $t_{pd}$ | LDCK↑ | Any Q | | 18 | 26 | | 30 | ns |
| $t_{pd}$ | UNCK↑ | Any Q | | 18 | 24 | | 27 | ns |
| $t_{PLH}$ | LDCK↑ | $\overline{EMPTY}$ | | 12 | 16 | | 18 | ns |
| $t_{PHL}$ | UNCK↑ | $\overline{EMPTY}$ | | 12 | 17 | | 20 | ns |
| $t_{PHL}$ | RST↓ | $\overline{EMPTY}$ | | 12 | 17 | | 20 | ns |
| $t_{PHL}$ | LDCK↑ | $\overline{FULL}$ | | 16 | 21 | | 22 | ns |
| $t_{PLH}$ | UNCK↑ | $\overline{FULL}$ | | 10 | 15 | | 18 | ns |
| $t_{PLH}$ | $\overline{RST}$↓ | $\overline{FULL}$ | | 13 | 19 | | 23 | ns |
| $t_{PLH}$ | LDCK↑ | ALMOST FULL/EMPTY | | 22 | 27 | | 30 | ns |
| $t_{PHL}$ | | | | 19 | 25 | | 28 | |
| $t_{PLH}$ | UNCK↑ | ALMOST FULL/EMPTY | | 22 | 27 | | 30 | ns |
| $t_{PHL}$ | | | | 17 | 23 | | 26 | |
| $t_{PLH}$ | $\overline{RST}$↓ | ALMOST FULL/EMPTY | | 12 | 16 | | 18 | |
| $t_{PLH}$ | LDCK↑ | HALF FULL | | 22 | 27 | | 30 | ns |
| $t_{PHL}$ | $\overline{RST}$↓ | HALF FULL | | 28 | 32 | | 35 | ns |
| $t_{PHL}$ | UNCK↑ | HALF FULL | | 16 | 22 | | 25 | ns |
| $t_{en}$ | OE↑ | Q | | 11 | 15 | | 17 | ns |
| $t_{dis}$ | OE↓ | Q | | 11 | 17 | | 19 | ns |

- **Reads and Writes May Be Asynchronous or Coincident**
- **Organization:**
  - **SN74ACT7200L – 256 × 9**
  - **SN74ACT7201LA – 512 × 9**
  - **SN74ACT7202LA – 1K × 9**
- **Fast Data Access Times of 15 ns**
- **Read and Write Frequencies up to 40 MHz**
- **Bit-Width and Word-Depth Expansion**
- **Fully Compatible With the IDT7200/7201/7202**
- **Retransmit Capability**
- **Empty, Full, and Half-Full Flags**
- **TTL-Compatible Inputs**

**DV OR NP PACKAGE**
**(TOP VIEW)**




**RJ PACKAGE**
**(TOP VIEW)**




NC – No internal connection

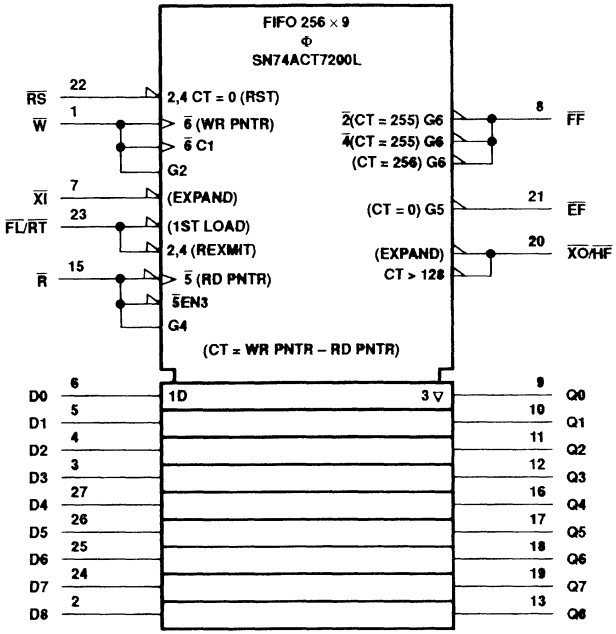
## description

The SN74ACT7200L, SN74ACT7201LA, and SN74ACT7202LA are constructed with dual-port SRAM and have internal write and read address counters to provide data throughput on a first-in, first-out (FIFO) basis. Write and read operations are independent and may be asynchronous or coincident. Empty and full status flags prevent underflow and overflow of memory, and depth expansion logic allows combining the storage cells of two or more devices into one FIFO. Word-width expansion is also possible.

Data is loaded into memory by the write enable ($\overline{W}$) input and unloaded by the read enable ($\overline{R}$) input. Read and write cycle times of 25 ns (40 MHz) are possible with data access times of 15 ns.

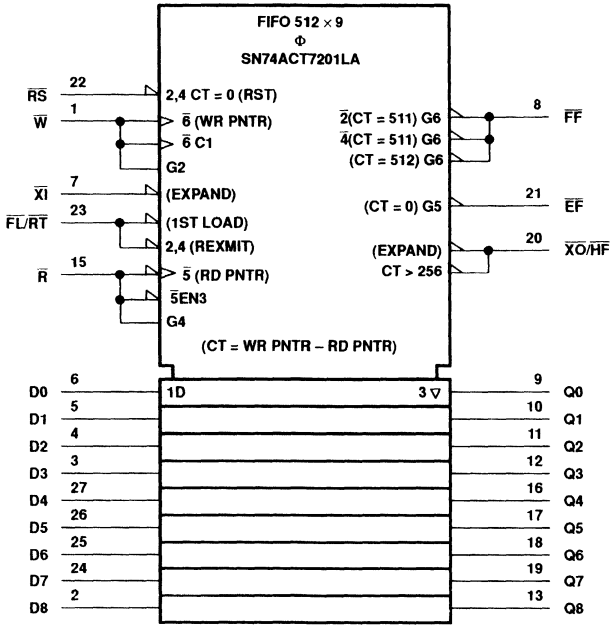
These devices are particularly suited for providing a data channel between two buses operating at asynchronous rates. Applications include use as rate buffers from analog-to-digital converters in data acquisition systems, temporary storage elements between buses and magnetic or optical memories, and queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information. The read pointer can be reset independently of the write pointer for retransmitting previously read data when a device is not used in depth expansion.

## SN74ACT7200L logic symbol†



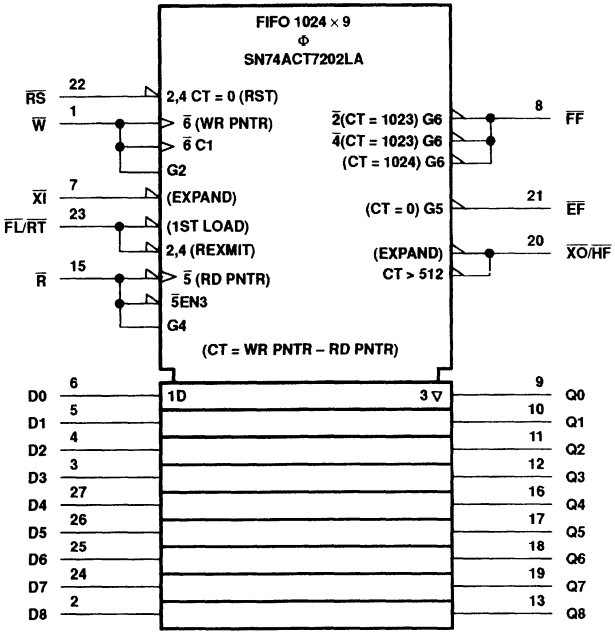

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

## SN74ACT7201LA logic symbol†



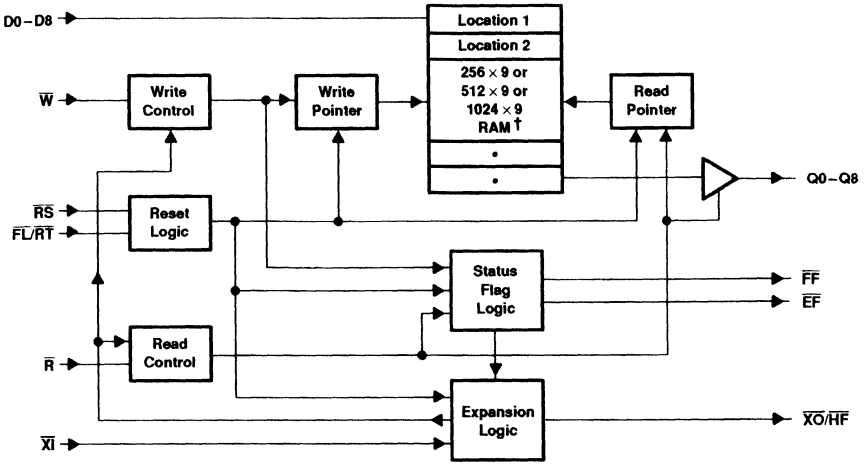

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

## SN74ACT7202LA logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

## functional block diagram




† 256 × 9 for SN74ACT7200L; 512 × 9 for SN74ACT7201LA; 1024 × 9 for SN74ACT7202LA

**RESET AND RETRANSMIT FUNCTION TABLE**
**(Single Device Depth; Single or Multiple Device Width)**

| INPUTS | | | INTERNAL TO DEVICE | | OUTPUTS | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{RS}$ | $\overline{FL/RT}$ | $\overline{XI}$ | READ POINTER | WRITE POINTER | $\overline{EF}$ | $\overline{FF}$ | $\overline{XO/HF}$ | |
| L | X | L | Location zero | Location zero | L | H | H | Reset device |
| H | L | L | Location zero | Unchanged | X | X | X | Retransmit |
| H | H | L | Increment if $\overline{EF}$ high | Increment if $\overline{FF}$ high | X | X | X | Read/write |

**RESET AND FIRST-LOAD FUNCTION TABLE**
**(Multiple Device Depth; Single or Multiple Device Width)**

| INPUTS | | | INTERNAL TO DEVICE | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|---|---|
| $\overline{RS}$ | $\overline{FL/RT}$ | $\overline{XI}$ | READ POINTER | WRITE POINTER | $\overline{EF}$ | $\overline{FF}$ | |
| L | L | ‡ | Location zero | Location zero | L | H | Reset first device |
| L | H | ‡ | Location zero | Location zero | L | H | Reset all other devices |
| H | X | ‡ | X | X | X | X | Read/write |

‡ $\overline{XI}$ is connected to $\overline{XO/HF}$ of the previous device in the daisy chain (see Figure 16).

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| D0–D8 | I | Data inputs |
| $\overline{EF}$ | O | Empty flag output. The empty flag output is low when the read pointer is equal to the write pointer, inhibiting any operation initiated by a read cycle. When the FIFO is empty, a data word can be read automatically at the data (Q0–Q8) outputs by holding the read enable ($\overline{R}$) input low when loading the data word with a low-level pulse on the write enable ($\overline{W}$) input. |
| $\overline{FF}$ | O | Full flag output. The full flag output is low when the write pointer is one location less than the read pointer, indicating the device is full and inhibiting any operation initiated by a write cycle. $\overline{FF}$ goes low when the number of writes after reset exceeds the number of reads by 256 for the SN74ACT7200L, 512 for the SN74ACT7201LA, and 1024 for the SN74ACT7202LA. When the FIFO is full, a data word can be written automatically into memory by holding the write enable ($\overline{W}$) input low while reading out another data word with a low-level pulse on the read enable ($\overline{R}$) input. |
| $\overline{FL}/\overline{RT}$ | I | First load/retransmit input. This input performs two separate functions. When cascading two or more devices for word-depth expansion, the $\overline{FL}/\overline{RT}$ input is tied to ground on the first device in the daisy chain to indicate that it is the first device loaded and unloaded; it is tied high on all other devices in the depth expansion chain.<br><br>A device is not used in depth expansion when its expansion ($\overline{XI}$) input is tied to ground, in which case the $\overline{FL}/\overline{RT}$ input acts as a retransmit enable. A retransmit operation is initiated when $\overline{FL}/\overline{RT}$ is pulsed low. This sets the internal read pointer to the first location and does not affect the write pointer. The read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be at a high logic level during the low-level $\overline{FL}/\overline{RT}$ retransmit pulse. Retransmit should be used only when less than 256/512/1024 writes are performed between resets, otherwise an attempt to retransmit may cause the loss of unread data. The retransmit function can affect the expansion-out/half-full flag output ($\overline{HF}$) depending on the relative locations of the read and write pointers. |
| GND | | Ground |
| Q0–Q8 | O | Data outputs. These outputs are in the high-impedance state when the read enable ($\overline{R}$) input is high or the FIFO is empty. |
| $\overline{R}$ | I | Read enable input. A read cycle begins on the falling edge of the read enable input if the empty flag ($\overline{EF}$) output is high. This activates the data (Q0–Q8) outputs and shifts the next data value to this bus. The data outputs return to the high-impedance state as $\overline{R}$ goes high. As the last stored word is read by the falling edge of $\overline{R}$, the empty flag ($\overline{EF}$) output transitions low, but the Q0–Q8 outputs remain active until $\overline{R}$ returns high. When the FIFO is empty, the internal read pointer is unchanged by a pulse on $\overline{R}$. |
| $\overline{RS}$ | I | Reset input. A reset is performed by taking the reset input low. This initializes the internal read and write pointers to the first location and sets the empty flag ($\overline{EF}$) output low, the full flag ($\overline{FF}$) output high, and the half-full flag ($\overline{HF}$) output high. Both the read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be held high for a reset during the window shown in Figure 7. A reset is required after power up before a write operation can take place. |
| $V_{CC}$ | | Supply voltage |
| $\overline{W}$ | I | Write enable input. A write cycle begins on the falling edge of the write enable input if the full flag ($\overline{FF}$) output is high. The value on the data (D0–D8) inputs is stored in memory as $\overline{W}$ returns high. When the FIFO is full, $\overline{FF}$ is low, inhibiting the write enable ($\overline{W}$) input from performing any operation on the device. |
| $\overline{XI}$ | I | Expansion in input. This input performs two functions. $\overline{XI}$ is tied to ground to indicate that the device is not used in depth expansion. When the device is used in depth expansion, its $\overline{XI}$ input is connected to the expansion out ($\overline{XO}$) output of the previous device in the depth-expansion chain. |
| $\overline{XO}/\overline{HF}$ | O | Expansion-out/half-full-flag output. This output performs two functions. When the device is not used in depth expansion (i.e., when its $\overline{XI}$ input is tied to ground), this output indicates when half the memory locations are filled. After half of the memory is filled, the falling edge on the write enable ($\overline{W}$) input for the next write operation drives $\overline{XO}/\overline{HF}$ low. $\overline{XO}/\overline{HF}$ remains low until a rising edge of the read enable ($\overline{R}$) input reduces the number of words stored to exactly half of the total memory.<br><br>When the device is used in depth expansion, its $\overline{XO}/\overline{HF}$ output is connected to the expansion-in ($\overline{XI}$) input of the next device in the daisy chain. The $\overline{XO}/\overline{HF}$ output drives the daisy chain by sending a pulse to the next device when the previous device reaches the last memory location. |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (any input), $V_I$ . . . . . −0.5 V to 7 V
Continuous output current, $I_O$ . . . . . 50 mA
Voltage applied to a disabled three-state output . . . . . 5.5 V
Storage temperature range . . . . . −55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $\overline{XI}$ | 2.6 | | | V |
| | | Other inputs | 2 | | | |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −2 | mA |
| $I_{OL}$ | Low-level output current | | | | 8 | mA |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5.5 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2 mA | | 2.4 | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_{OZH}$ | $V_O = V_{CC}$, | $R \geq V_{IH}$ | | | ±10 | µA |
| $I_{OZL}$ | $V_O$ = 0.4 V, | $R \geq V_{IH}$ | | | ±10 | µA |
| $I_I$ | $V_I$ = 0 to 5.5 V | | | −1 | 1 | µA |
| $C_i$‡ | $V_I$ = 0, | $T_A$ = 25°C, | f = 1 MHz | | 8 | pF |
| $C_o$‡ | $V_O$ = 0, | $T_A$ = 25°C, | f = 1 MHz | | 8 | pF |

‡ This parameter is sampled and not 100% tested.

| PARAMETER | | TEST CONDITIONS | $t_a$ = 15 and 25 ns | | | $t_a$ = 50 ns | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{CC1}$§ | Supply current | | | | 125¶ | | 50 | 80 | mA |
| $I_{CC2}$§ | Standby current | $\overline{R}$, $\overline{W}$, $\overline{RS}$, and $\overline{FL}/\overline{RT}$ at $V_{IH}$ | | | 15 | | 5 | 8 | mA |
| $I_{CC3}$§ | Power-down current | $V_I = V_{CC}$ − 0.2 V | | | 0.5 | | | 0.5 | mA |

§ $I_{CC}$ measurements are made with outputs open (only capacitive loading).
¶ Tested at $f_{clock}$ = 20 MHz

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| | | FIGURE | 'ACT7200L15 'ACT7201LA15 'ACT7202LA15 | | 'ACT7200L25 'ACT7201LA25 'ACT7202LA25 | | 'ACT7200L50 'ACT7201LA50 'ACT7202LA50 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency, $\overline{R}$ or $\overline{W}$ | | | 40 | | 28.5 | | 15 | MHz |
| $t_{c(R)}$ | Cycle time, read | 1(a) | 25 | | 35 | | 65 | | ns |
| $t_{c(W)}$ | Cycle time, write | 1(b) | 25 | | 35 | | 65 | | ns |
| $t_{c(RS)}$ | Cycle time, reset | 7 | 25 | | 35 | | 65 | | ns |
| $t_{c(RT)}$ | Cycle time, retransmit | 4 | 25 | | 35 | | 65 | | ns |
| $t_{w(RL)}$ | Pulse duration, $\overline{R}$ low | 1(a) | 15 | | 25 | | 50 | | ns |
| $t_{w(WL)}$ | Pulse duration, $\overline{W}$ low | 1(b) | 15 | | 25 | | 50 | | ns |
| $t_{w(RH)}$ | Pulse duration, $\overline{R}$ high | 1(a) | 10 | | 10 | | 15 | | ns |
| $t_{w(WH)}$ | Pulse duration, $\overline{W}$ high | 1(b) | 10 | | 10 | | 15 | | ns |
| $t_{w(RT)}$ | Pulse duration, $\overline{FL}/\overline{RT}$ low | 4 | 15 | | 25 | | 50 | | ns |
| $t_{w(RS)}$ | Pulse duration, $\overline{RS}$ low | 7 | 15 | | 25 | | 50 | | ns |
| $t_{w(XIL)}$ | Pulse duration, $\overline{XI}$ low | 10 | 15 | | 25 | | 50 | | ns |
| $t_{w(XIH)}$ | Pulse duration, $\overline{XI}$ high | 10 | 10 | | 10 | | 10 | | ns |
| $t_{su(D)}$ | Setup time, data before $\overline{W}\uparrow$ | 1(b), 6 | 11 | | 15 | | 30 | | ns |
| $t_{su(RT)}$ | Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{FL}/\overline{RT}\uparrow$† | 4 | 15 | | 25 | | 50 | | ns |
| $t_{su(RS)}$ | Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{RS}\uparrow$† | 7 | 15 | | 25 | | 50 | | ns |
| $t_{su(XI\text{-}R)}$ | Setup time, $\overline{XI}$ low before $\overline{R}\downarrow$ | 10 | 10 | | 10 | | 15 | | ns |
| $t_{su(XI\text{-}W)}$ | Setup time, $\overline{XI}$ low before $\overline{W}\downarrow$ | 10 | 10 | | 10 | | 15 | | ns |
| $t_{h(D)}$ | Hold time, data after $\overline{W}\uparrow$ | 1(b), 6 | 0 | | 0 | | 5 | | ns |
| $t_{h(E\text{-}R)}$ | Hold time, $\overline{R}$ low after $\overline{EF}\uparrow$ | 5, 11 | 15 | | 25 | | 50 | | ns |
| $t_{h(F\text{-}W)}$ | Hold time, $\overline{W}$ low after $\overline{FF}\uparrow$ | 6, 12 | 15 | | 25 | | 50 | | ns |
| $t_{h(RT)}$ | Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{FL}/\overline{RT}\uparrow$ | 4 | 10 | | 10 | | 15 | | ns |
| $t_{h(RS)}$ | Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{RS}\uparrow$ | 7 | 10 | | 10 | | 15 | | ns |

† These values are characterized but not currently tested.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | | FIGURE | 'ACT7200L15 'ACT7201LA15 'ACT7202LA15 | | 'ACT7200L25 'ACT7201LA25 'ACT7202LA25 | | 'ACT7200L50 'ACT7201LA50 'ACT7202LA50 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | Clock frequency, $\overline{R}$ or $\overline{W}$ | | 40 | | 28.5 | | 15 | | MHz |
| $t_a$ | Access time, $\overline{R}\downarrow$ or $\overline{EF}\uparrow$ to data out valid | 1(a), 3, 5 | | 15 | | 25 | | 50 | ns |
| $t_{v(RH)}$ | Valid time, data out valid after $\overline{R}\uparrow$ | 1(a) | 5 | | 5 | | 5 | | ns |
| $t_{en(R\text{-}QX)}$ | Enable time, $\overline{R}\downarrow$ to Q outputs at low impedance† | 1(a) | 5 | | 5 | | 10 | | ns |
| $t_{en(W\text{-}QX)}$ | Enable time, $\overline{W}\uparrow$ to Q outputs at low impedance†‡ | 5 | 5 | | 5 | | 15 | | ns |
| $t_{dis(R)}$ | Disable time, $\overline{R}\uparrow$ to Q outputs at high impedance† | 1(a) | | 15 | | 18 | | 30 | ns |
| $t_{w(FH)}$ | Pulse duration, $\overline{FF}$ high in automatic write mode | 6 | | 15 | | 25 | | 45 | ns |
| $t_{w(EH)}$ | Pulse duration, $\overline{EF}$ high in automatic read mode | 5 | | 15 | | 25 | | 45 | ns |
| $t_{p(W\text{-}F)}$ | Propagation delay time, $\overline{W}\downarrow$ to $\overline{FF}$ low | 2 | | 15 | | 25 | | 45 | ns |
| $t_{p(R\text{-}F)}$ | Propagation delay time, $\overline{R}\uparrow$ to $\overline{FF}$ high | 2, 6, 12 | | 15 | | 25 | | 45 | ns |
| $t_{p(RS\text{-}F)}$ | Propagation delay time, $\overline{RS}\downarrow$ to $\overline{FF}$ high | 7 | | 25 | | 35 | | 65 | ns |
| $t_{p(RS\text{-}HF)}$ | Propagation delay time, $\overline{RS}\downarrow$ to $\overline{XO}/\overline{HF}$ high | 7 | | 25 | | 35 | | 65 | ns |
| $t_{p(W\text{-}E)}$ | Propagation delay time, $\overline{W}\uparrow$ to $\overline{EF}$ high | 3, 5, 11 | | 15 | | 25 | | 45 | ns |
| $t_{p(R\text{-}E)}$ | Propagation delay time, $\overline{R}\downarrow$ to $\overline{EF}$ low | 3 | | 15 | | 25 | | 45 | ns |
| $t_{p(RS\text{-}E)}$ | Propagation delay time, $\overline{RS}\downarrow$ to $\overline{EF}$ low | 7 | | 25 | | 35 | | 65 | ns |
| $t_{p(W\text{-}HF)}$ | Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO}/\overline{HF}$ low | 8 | | 25 | | 35 | | 65 | ns |
| $t_{p(R\text{-}HF)}$ | Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO}/\overline{HF}$ high | 8 | | 25 | | 35 | | 65 | ns |
| $t_{p(R\text{-}XOL)}$ | Propagation delay time, $\overline{R}\downarrow$ to $\overline{XO}/\overline{HF}$ low | 9 | | 15 | | 25 | | 50 | ns |
| $t_{p(W\text{-}XOL)}$ | Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO}/\overline{HF}$ low | 9 | | 15 | | 25 | | 50 | ns |
| $t_{p(R\text{-}XOH)}$ | Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO}/\overline{HF}$ high | 9 | | 15 | | 25 | | 50 | ns |
| $t_{p(W\text{-}XOH)}$ | Propagation delay time, $\overline{W}\uparrow$ to $\overline{XO}/\overline{HF}$ high | 9 | | 15 | | 25 | | 50 | ns |
| $t_{p(RT\text{-}FL)}$ | Propagation delay time, $\overline{FL}/\overline{RT}\downarrow$ to $\overline{HF}$, $\overline{EF}$, $\overline{FF}$ valid | 4 | | 25 | | 35 | | 65 | ns |

† These values are characterized but not currently tested.
‡ Only applies when data is automatically read (see Figure 5)

## PARAMETER MEASUREMENT INFORMATION

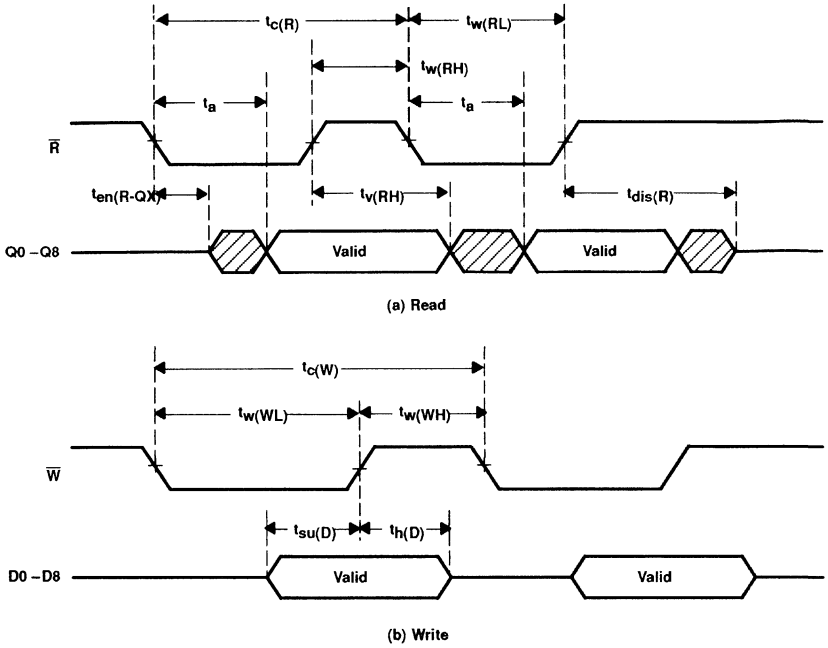



Figure 1. Asynchronous Waveforms

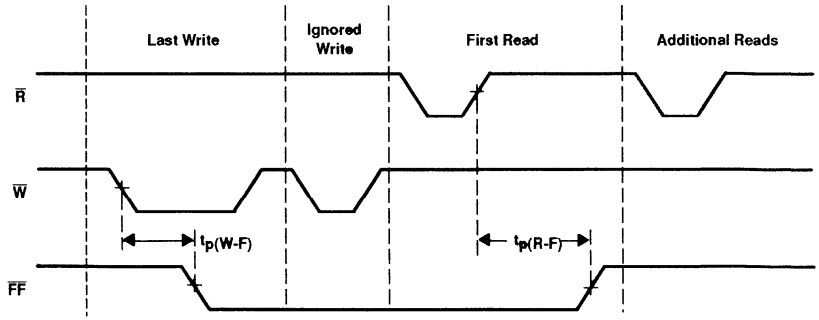



Figure 2. Full Flag Waveforms

## PARAMETER MEASUREMENT INFORMATION

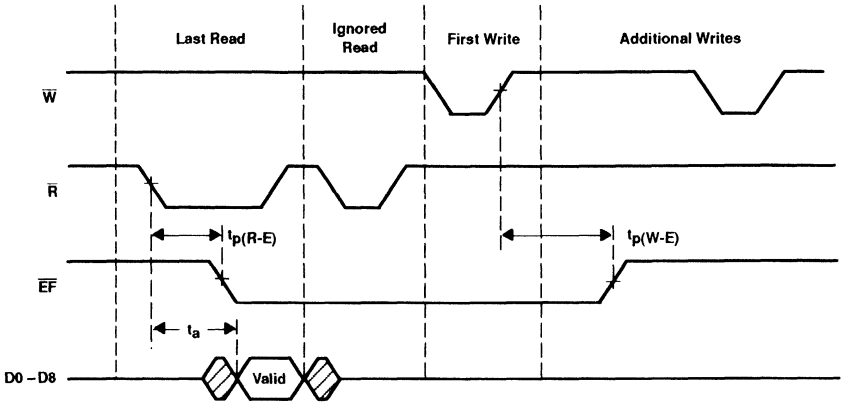



**Figure 3. Empty Flag Waveforms**

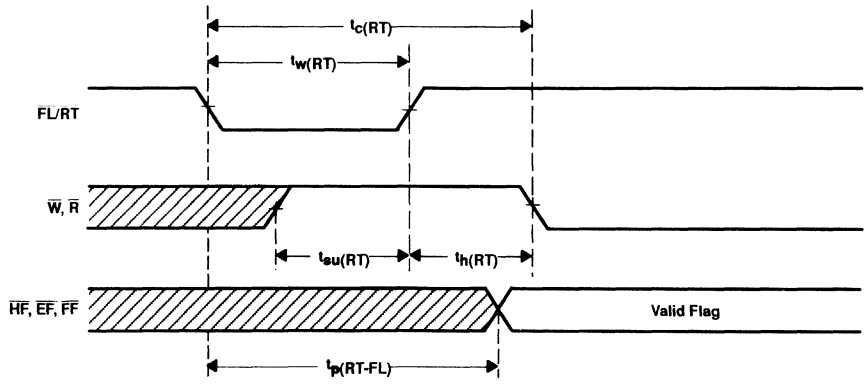



**Figure 4. Retransmit Waveforms (see Note 2)**

NOTE 2: The $\overline{EF}$, $\overline{FF}$, and $\overline{XO}/\overline{HF}$ status flags will be valid after completion of the retransmit cycle.

## PARAMETER MEASUREMENT INFORMATION

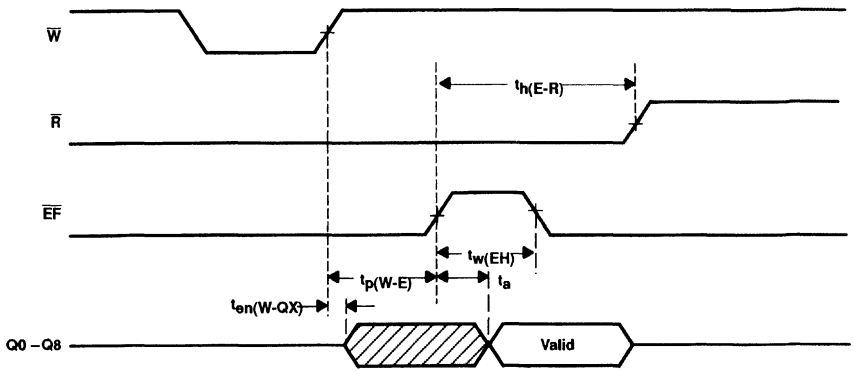



Figure 5. Automatic Read Waveforms

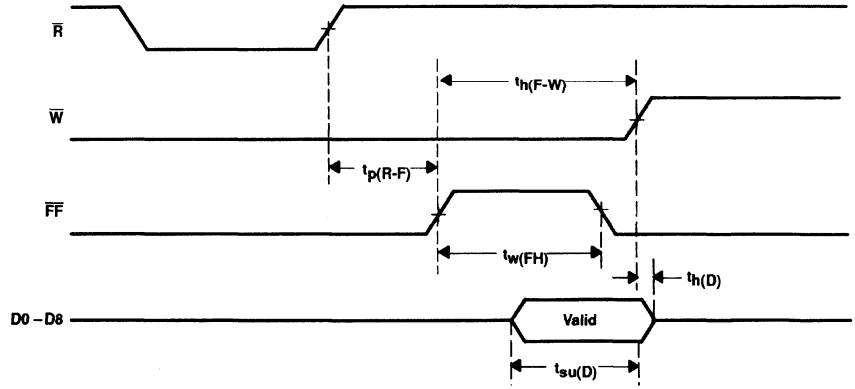



Figure 6. Automatic Write Waveforms

## PARAMETER MEASUREMENT INFORMATION

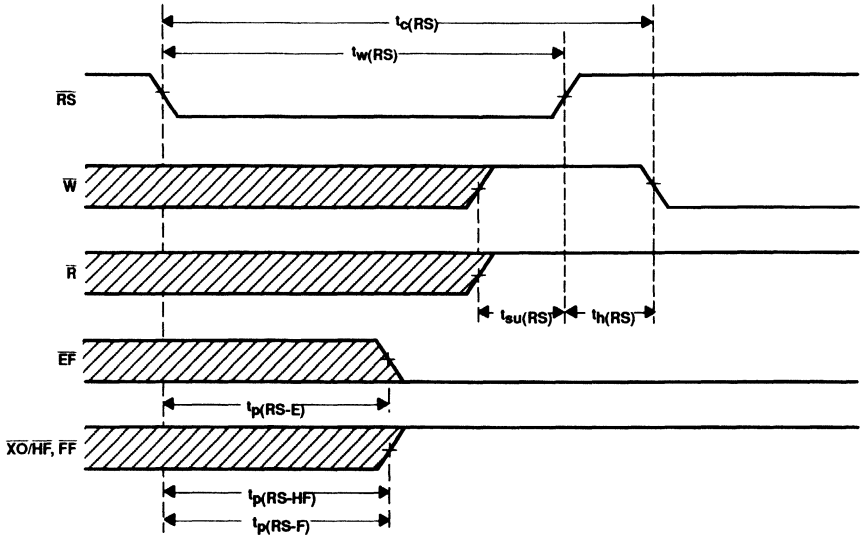



Figure 7. Master Reset Waveforms

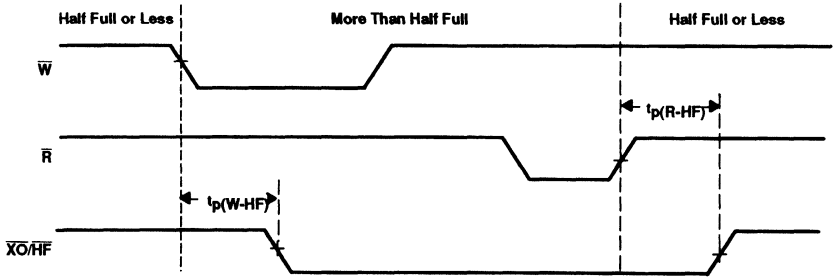



Figure 8. Half-Full Flag Waveforms

## PARAMETER MEASUREMENT INFORMATION

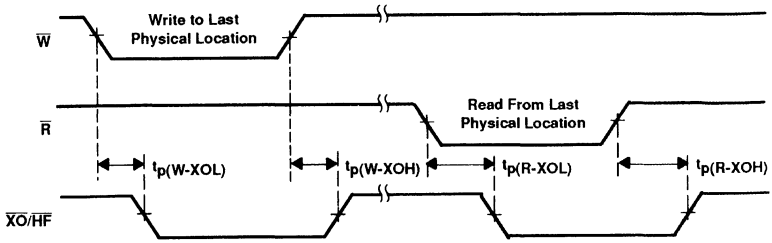



Figure 9. Expansion-Out Waveforms

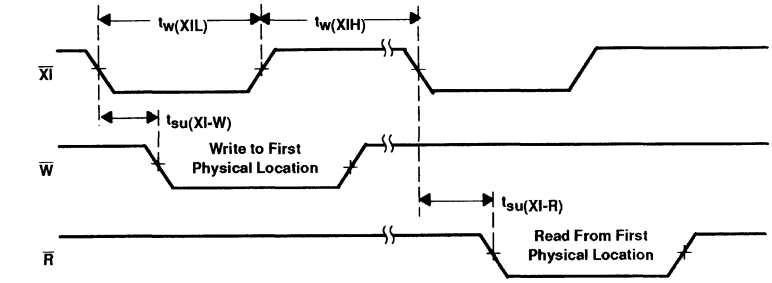



Figure 10. Expansion-In Waveforms

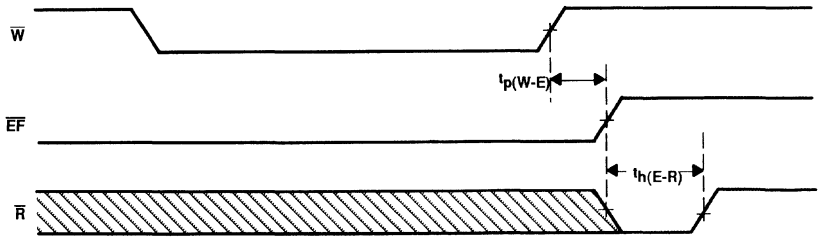



Figure 11. Minimum Timing for an Empty Flag Coincident Read Pulse

## PARAMETER MEASUREMENT INFORMATION

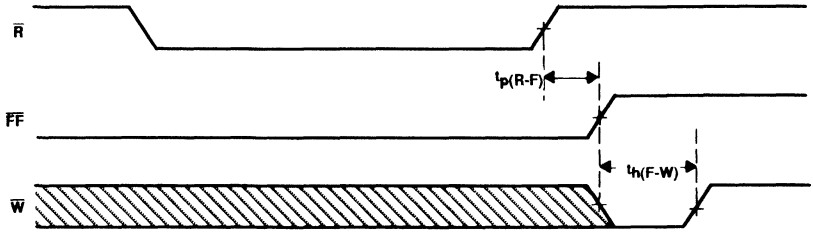



**Figure 12. Minimum Timing for a Full Flag Coincident Write Pulse**

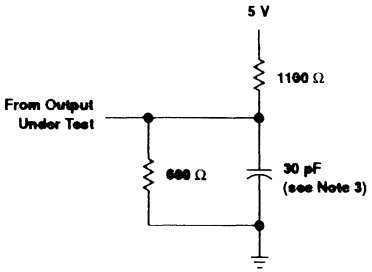



**Figure 13. Load Circuit**

NOTE 3: Includes probe and jig capacitance

## PARAMETER MEASUREMENT INFORMATION

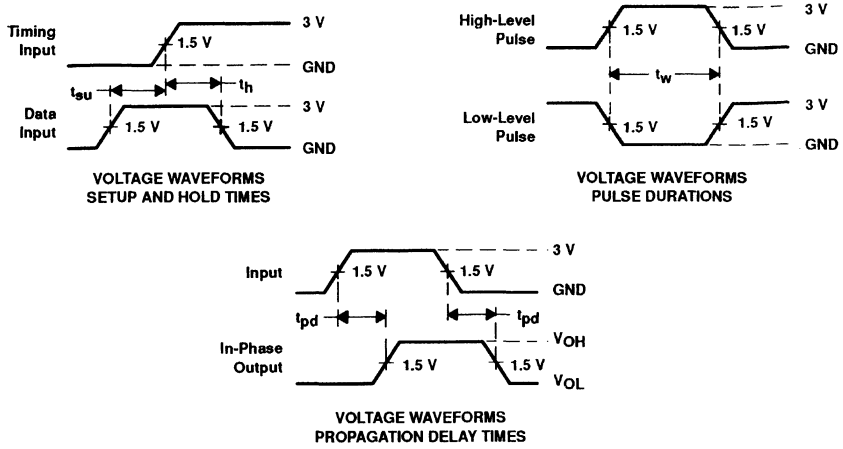



**Figure 14. Timing Reference Levels**

## APPLICATION INFORMATION

Combining two or more devices to create one FIFO with a greater number of memory bits is accomplished in two different ways. Width expansion increases the number of bits in each word by connecting FIFOs with the same depth in parallel. Depth expansion uses the built-in expansion logic to daisy-chain two or more devices for applications requiring more than 256, 512, or 1024 words of storage. Width expansion and depth expansion can be used together.

### width expansion

Word-width expansion is achieved by connecting the corresponding input control to multiple devices with the same depth. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be monitored from any one device. Figure 15 shows two FIFOs in a width-expansion configuration. Note that both devices have their expansion in ($\overline{XI}$) inputs tied to ground. This disables the depth-expansion function of the device, allowing the first load/retransmit ($\overline{FL}/\overline{RT}$) input to function as a retransmit ($\overline{RT}$) input and the expansion out/half-full ($\overline{XO}/\overline{HF}$) output to function as a half-full ($\overline{HF}$) flag.

### depth expansion

The SN74ACT7200L/7201LA/7202LA is easily expanded in depth. Figure 16 shows the connections used to depth expand three SN74ACT7200L/7201LA/7202LA devices. Any depth can be attained by adding additional devices to the chain. The SN74ACT7200L/7201LA/7202LA operates in depth expansion under the following conditions (see Figure 16):

1. The first device in the chain is designated by tying the first load ($\overline{FL}$) input to ground.
2. All other devices must have their $\overline{FL}$ inputs at a high logic level.
3. The expansion out ($\overline{XO}$) output of each device must be tied to the expansion in ($\overline{XI}$) input of the next device.
4. External logic is needed to generate a composite full flag ($\overline{FF}$) and empty flag ($\overline{EF}$) (all $\overline{FF}$ outputs must be ORed together, and all $\overline{EF}$ outputs must be ORed together).
5. The retransmit ($\overline{RT}$) and half-full ($\overline{HF}$) functions are not available in the depth-expanded configuration.

### combined depth and width expansion

Both expansion techniques can be used together to increase depth and width. This is done by first creating depth-expanded units and then connecting them in a width-expanded configuration (see Figure 17).

## APPLICATION INFORMATION

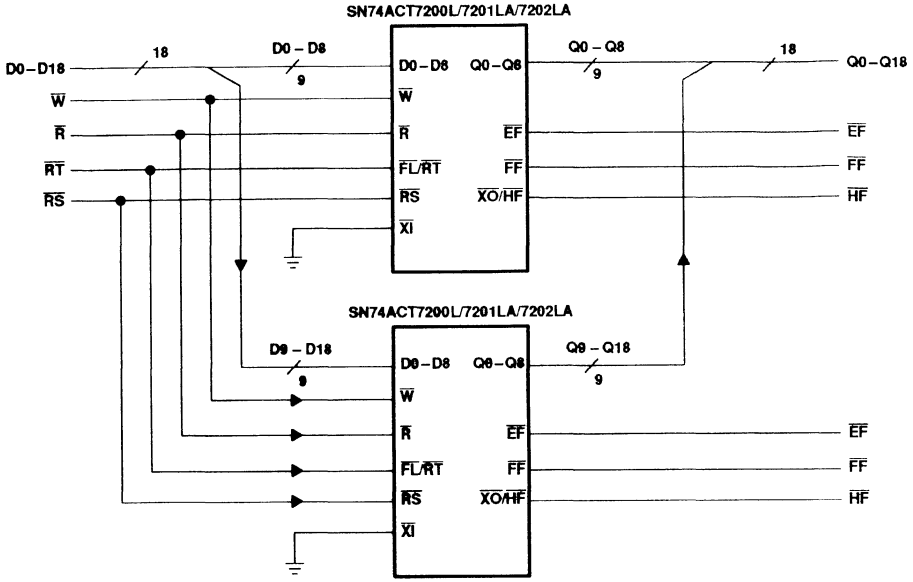



Figure 15. Word-Width Expansion: 256/512/1024-Word By 18-Bit

## APPLICATION INFORMATION

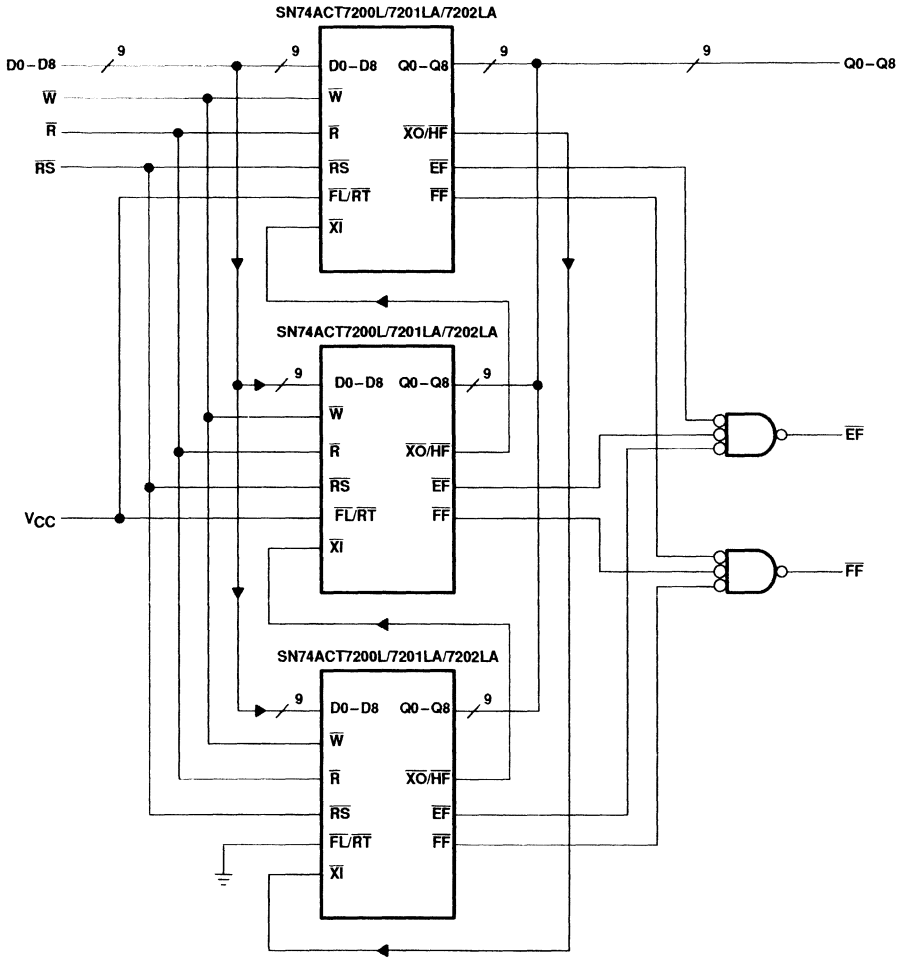



Figure 16. Word-Depth Expansion: 768 × 9/1536 × 9/3072 × 9 FIFO Memory

## APPLICATION INFORMATION

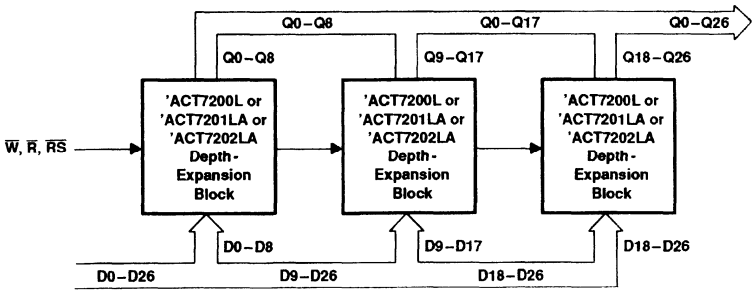
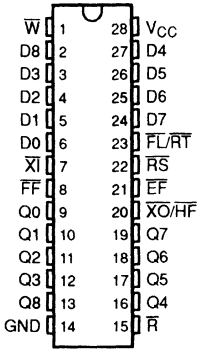


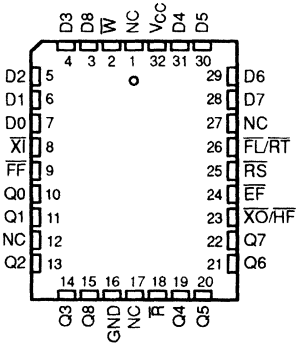

Figure 17. Word-Depth Plus Word-Width Expansion

- **Reads and Writes May Be Asynchronous or Coincident**
- **Organization:**
  - **SN74ACT7203L – 2048 × 9**
  - **SN74ACT7204L – 4096 × 9**
- **Fast Data Access Times of 15 ns**
- **Read and Write Frequencies up to 40 MHz**
- **Bit-Width and Word-Depth Expansion**
- **Fully Compatible With the IDT7203/7204**
- **Retransmit Capability**
- **Empty, Full, and Half-Full Flags**
- **TTL-Compatible Inputs**

**NP PACKAGE**
**(TOP VIEW)**




**RJ PACKAGE**
**(TOP VIEW)**




NC – No internal connection

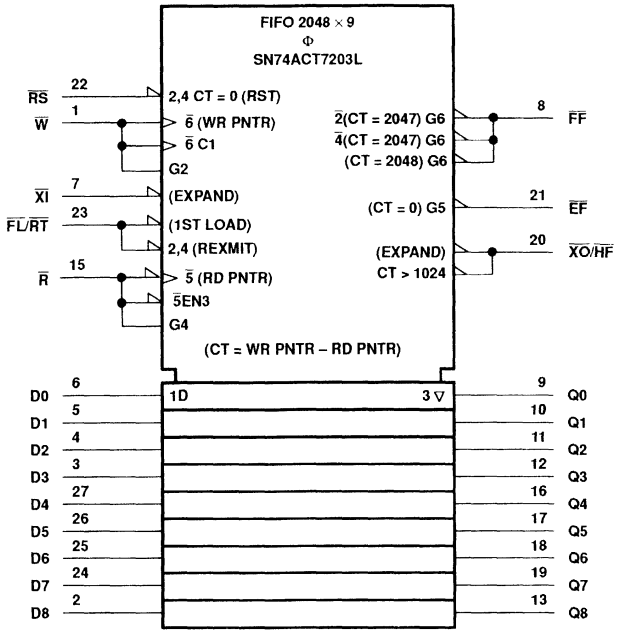
## description

The SN74ACT7203L and SN74ACT7204L are constructed with dual-port SRAM and have internal write and read address counters to provide data throughput on a first-in, first-out (FIFO) basis. Write and read operations are independent and may be asynchronous or coincident. Empty and full status flags prevent underflow and overflow of memory, and depth expansion logic allows combining the storage cells of two or more devices into one FIFO. Word-width expansion is also possible.

Data is loaded into memory by the write enable ($\overline{W}$) input and unloaded by the read enable ($\overline{R}$) input. Read and write cycle times of 25 ns (40 MHz) are possible with data access times of 15 ns.

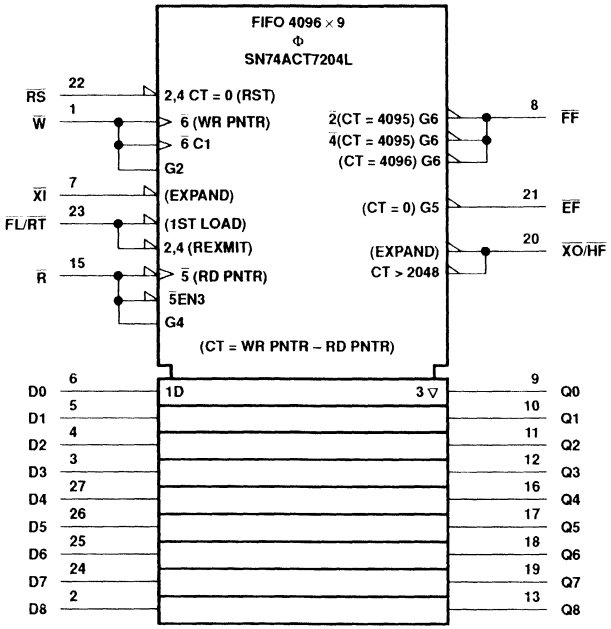
These devices are particularly suited for providing a data channel between two buses operating at asynchronous rates. Applications include use as rate buffers from analog-to-digital converters in data acquisition systems, temporary storage elements between buses and magnetic or optical memories, and queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information. The read pointer can be reset independently of the write pointer for retransmitting previously read data when a device is not used in depth expansion.

## SN74ACT7203L logic symbol†



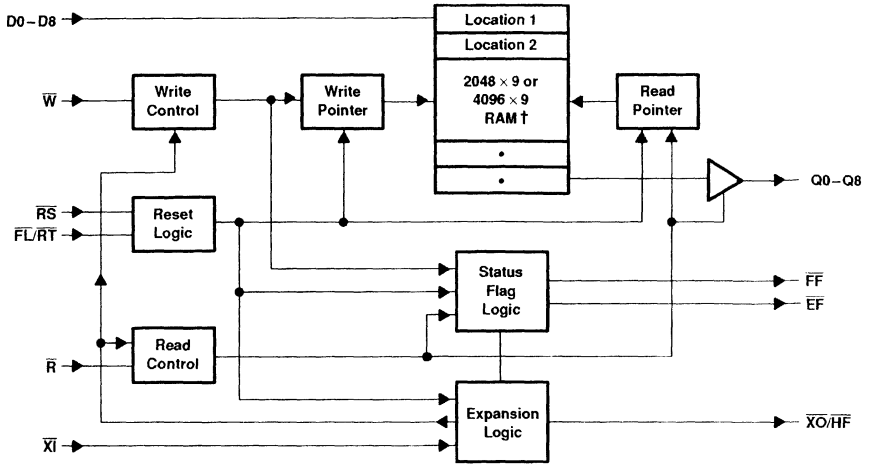

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the NP package.

## SN74ACT7204L logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the NP package.

## functional block diagram




† 2048 × 9 for SN74ACT7203L; 4096 × 9 for SN74ACT7204L

**RESET AND RETRANSMIT FUNCTION TABLE**
**(Single Device Depth; Single or Multiple Device Width)**

| INPUTS | | | INTERNAL TO DEVICE | | OUTPUTS | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{RS}$ | $\overline{FL}/\overline{RT}$ | $\overline{XI}$ | READ POINTER | WRITE POINTER | $\overline{EF}$ | $\overline{FF}$ | $\overline{XO}/\overline{HF}$ | |
| L | X | L | Location zero | Location zero | L | H | H | Reset device |
| H | L | L | Location zero | Unchanged | X | X | X | Retransmit |
| H | H | L | Increment if $\overline{EF}$ high | Increment if $\overline{FF}$ high | X | X | X | Read/write |

**RESET AND FIRST-LOAD FUNCTION TABLE**
**(Multiple Device Depth; Single or Multiple Device Width)**

| INPUTS | | | INTERNAL TO DEVICE | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|---|---|
| $\overline{RS}$ | $\overline{FL}/\overline{RT}$ | $\overline{XI}$ | READ POINTER | WRITE POINTER | $\overline{EF}$ | $\overline{FF}$ | |
| L | L | ‡ | Location zero | Location zero | L | H | Reset first device |
| L | H | ‡ | Location zero | Location zero | L | H | Reset all other devices |
| H | X | ‡ | X | X | X | X | Read/write |

‡ $\overline{XI}$ is connected to $\overline{XO}/\overline{HF}$ of the previous device in the daisy chain (see Figure 16).

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| D0–D8 | I | Data inputs |
| $\overline{EF}$ | O | Empty flag output. The empty flag output is low when the read pointer is equal to the write pointer, inhibiting any operation initiated by a read cycle. When the FIFO is empty, a data word can be read automatically at the data (Q0–Q8) outputs by holding the read enable ($\overline{R}$) input low when loading the data word with a low-level pulse on the write enable ($\overline{W}$) input. |
| $\overline{FF}$ | O | Full flag output. The full flag output is low when the write pointer is one location less than the read pointer, indicating the device is full and inhibiting any operation initiated by a write cycle. $\overline{FF}$ goes low when the number of writes after reset exceeds the number of reads by 2048 for the SN74ACT7203L and 4096 for the SN74ACT7204L. When the FIFO is full, a data word can be written automatically into memory by holding the write enable ($\overline{W}$) input low while reading out another data word with a low-level pulse on the read enable ($\overline{R}$) input. |
| $\overline{FL}/\overline{RT}$ | I | First load/retransmit input. This input performs two separate functions. When cascading two or more devices for word-depth expansion, the $\overline{FL}/\overline{RT}$ input is tied to ground on the first device in the daisy chain to indicate that it is the first device loaded and unloaded; it is tied high on all other devices in the depth expansion chain.<br><br>A device is not used in depth expansion when its expansion ($\overline{XI}$) input is tied to ground, in which case the $\overline{FL}/\overline{RT}$ input acts as a retransmit enable. A retransmit operation is initiated when $\overline{FL}/\overline{RT}$ is pulsed low. This sets the internal read pointer to the first location and does not affect the write pointer. The read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be at a high logic level during the low-level $\overline{FL}/\overline{RT}$ retransmit pulse. Retransmit should be used only when less than 2048/4096 writes are performed between resets, otherwise an attempt to retransmit may cause the loss of unread data. The retransmit function can affect the expansion-out/half-full flag output ($\overline{HF}$) depending on the relative locations of the read and write pointers. |
| GND | | Ground |
| Q0–Q8 | O | Data outputs. These outputs are in the high-impedance state when the read enable ($\overline{R}$) input is high or the FIFO is empty. |
| $\overline{R}$ | I | Read enable input. A read cycle begins on the falling edge of the read enable input if the empty flag ($\overline{EF}$) output is high. This activates the data (Q0–Q8) outputs and shifts the next data value to this bus. The data outputs return to the high-impedance state as $\overline{R}$ goes high. As the last stored word is read by the falling edge of $\overline{R}$, the empty flag ($\overline{EF}$) output transitions low, but the Q0–Q8 outputs remain active until $\overline{R}$ returns high. When the FIFO is empty, the internal read pointer is unchanged by a pulse on $\overline{R}$. |
| $\overline{RS}$ | I | Reset input. A reset is performed by taking the reset input low. This initializes the internal read and write pointers to the first location and sets the empty flag ($\overline{EF}$) output low, the full flag ($\overline{FF}$) output high, and the half-full flag ($\overline{HF}$) output high. Both the read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be held high for a reset during the window shown in Figure 7. A reset is required after power up before a write operation can take place. |
| $V_{CC}$ | | Supply voltage |
| $\overline{W}$ | I | Write enable input. A write cycle begins on the falling edge of the write enable input if the full flag ($\overline{FF}$) output is high. The value on the data (D0–D8) inputs is stored in memory as $\overline{W}$ returns high. When the FIFO is full, $\overline{FF}$ is low, inhibiting the write enable ($\overline{W}$) input from performing any operation on the device. |
| $\overline{XI}$ | I | Expansion in input. This input performs two functions. $\overline{XI}$ is tied to ground to indicate that the device is not used in depth expansion. When the device is used in depth expansion, its $\overline{XI}$ input is connected to the expansion out ($\overline{XO}$) output of the previous device in the depth-expansion chain. |
| $\overline{XO}/\overline{HF}$ | O | Expansion-out/half-full-flag output. This output performs two functions. When the device is not used in depth expansion (i.e., when its $\overline{XI}$ input is tied to ground), this output indicates when half the memory locations are filled. After half of the memory is filled, the falling edge on the write enable ($\overline{W}$) input for the next write operation drives $\overline{XO}/\overline{HF}$ low. $\overline{XO}/\overline{HF}$ remains low until a rising edge of the read enable ($\overline{R}$) input reduces the number of words stored to exactly half of the total memory.<br><br>When the device is used in depth expansion, its $\overline{XO}/\overline{HF}$ output is connected to the expansion-in ($\overline{XI}$) input of the next device in the daisy chain. The $\overline{XO}/\overline{HF}$ output drives the daisy chain by sending a pulse to the next device when the previous device reaches the last memory location. |

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) ..... −0.5 V to 7 V
Input voltage range (any input), $V_I$ ..... −0.5 V to 7 V
Continuous output current, $I_O$ ..... 50 mA
Voltage applied to a disabled three-state output ..... 5.5 V
Storage temperature range ..... −55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $\overline{XI}$ | 2.6 | | | V |
| | | Other inputs | 2 | | | |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −2 | mA |
| $I_{OL}$ | Low-level output current | | | | 8 | mA |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5.5 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2 mA | | 2.4 | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_{OZH}$ | $V_O = V_{CC}$, | $\overline{R} \geq V_{IH}$ | | | ±10 | μA |
| $I_{OZL}$ | $V_O$ = 0.4 V, | $\overline{R} \geq V_{IH}$ | | | ±10 | μA |
| $I_I$ | $V_I$ = 0 to 5.5 V | | | −1 | 1 | μA |
| $I_{CC1}$§ | $f_{clock}$ = 20 MHz | | | | 120 | mA |
| $I_{CC2}$§ | $\overline{R}$, $\overline{W}$, $\overline{RS}$, and $\overline{FL}/\overline{RT}$ at $V_{IH}$ | | | | 12 | mA |
| $I_{CC3}$§ | $V_I = V_{CC} - 0.2$ V | | | | 2 | mA |
| $C_i$‡ | $V_I$ = 0, | $T_A$ = 25°C, | f = 1 MHz | | 10 | pF |
| $C_o$‡ | $V_O$ = 0, | $T_A$ = 25°C, | f = 1 MHz | | 10 | pF |

‡ This parameter is sampled and not 100% tested.

§ $I_{CC1}$ = supply current; $I_{CC2}$ = standby current; $I_{CC3}$ = power-down current. $I_{CC}$ measurements are made with outputs open (only capacitive loading).

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| | | FIGURE | 'ACT7203L25 'ACT7204L25 | | 'ACT7203L50 'ACT7204L50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency, $\overline{R}$ or $\overline{W}$ | | | 28.5 | | 15 | MHz |
| $t_{c(R)}$ | Cycle time, read | 1(a) | 35 | | 65 | | ns |
| $t_{c(W)}$ | Cycle time, write | 1(b) | 35 | | 65 | | ns |
| $t_{c(RS)}$ | Cycle time, reset | 7 | 35 | | 65 | | ns |
| $t_{c(RT)}$ | Cycle time, retransmit | 4 | 35 | | 65 | | ns |
| $t_{w(RL)}$ | Pulse duration, $\overline{R}$ low | 1(a) | 25 | | 50 | | ns |
| $t_{w(WL)}$ | Pulse duration, $\overline{W}$ low | 1(b) | 25 | | 50 | | ns |
| $t_{w(RH)}$ | Pulse duration, $\overline{R}$ high | 1(a) | 10 | | 15 | | ns |
| $t_{w(WH)}$ | Pulse duration, $\overline{W}$ high | 1(b) | 10 | | 15 | | ns |
| $t_{w(RT)}$ | Pulse duration, $\overline{FL/RT}$ low | 4 | 25 | | 50 | | ns |
| $t_{w(RS)}$ | Pulse duration, $\overline{RS}$ low | 7 | 25 | | 50 | | ns |
| $t_{w(XIL)}$ | Pulse duration, $\overline{XI}$ low | 10 | 25 | | 50 | | ns |
| $t_{w(XIH)}$ | Pulse duration, $\overline{XI}$ high | 10 | 10 | | 10 | | ns |
| $t_{su(D)}$ | Setup time, data before $\overline{W}\uparrow$ | 1(b), 6 | 15 | | 30 | | ns |
| $t_{su(RT)}$ | Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{FL/RT}\uparrow$† | 4 | 25 | | 50 | | ns |
| $t_{su(RS)}$ | Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{RS}\uparrow$† | 7 | 25 | | 50 | | ns |
| $t_{su(XI\text{-}R)}$ | Setup time, $\overline{XI}$ low before $\overline{R}\downarrow$ | 10 | 10 | | 15 | | ns |
| $t_{su(XI\text{-}W)}$ | Setup time, $\overline{XI}$ low before $\overline{W}\downarrow$ | 10 | 10 | | 15 | | ns |
| $t_{h(D)}$ | Hold time, data after $\overline{W}\uparrow$ | 1(b), 6 | 0 | | 5 | | ns |
| $t_{h(E\text{-}R)}$ | Hold time, $\overline{R}$ low after $\overline{EF}\uparrow$ | 5, 11 | 25 | | 50 | | ns |
| $t_{h(F\text{-}W)}$ | Hold time, $\overline{W}$ low after $\overline{FF}\uparrow$ | 6, 12 | 25 | | 50 | | ns |
| $t_{h(RT)}$ | Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{FL/RT}\uparrow$† | 4 | 10 | | 15 | | ns |
| $t_{h(RS)}$ | Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{RS}\uparrow$ | 7 | 10 | | 15 | | ns |

† These values are characterized but not currently tested.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | | FIGURE | 'ACT7203L25 'ACT7204L25 | | 'ACT7203L50 'ACT7204L50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | Clock frequency, $\overline{R}$ or $\overline{W}$ | | 28.5 | | 15 | | MHz |
| $t_a$ | Access time, $\overline{R}\downarrow$ or $\overline{EF}\uparrow$ to data out valid | 1(a), 3, 5 | | 25 | | 50 | ns |
| $t_{v(RH)}$ | Valid time, data out valid after $\overline{R}\uparrow$ | 1(a) | 5 | | 5 | | ns |
| $t_{en(R\text{-}QX)}$ | Enable time, $\overline{R}\downarrow$ to Q outputs at low impedance† | 1(a) | 5 | | 10 | | ns |
| $t_{en(W\text{-}QX)}$ | Enable time, $\overline{W}\uparrow$ to Q outputs at low impedance†‡ | 5 | 5 | | 15 | | ns |
| $t_{dis(R)}$ | Disable time, $\overline{R}\uparrow$ to Q outputs at high impedance† | 1(a) | | 18 | | 30 | ns |
| $t_{w(FH)}$ | Pulse duration, $\overline{FF}$ high in automatic write mode | 6 | | 25 | | 45 | ns |
| $t_{w(EH)}$ | Pulse duration, $\overline{EF}$ high in automatic read mode | 5 | | 25 | | 45 | ns |
| $t_{p(W\text{-}F)}$ | Propagation delay time, $\overline{W}\downarrow$ to $\overline{FF}$ low | 2 | | 25 | | 45 | ns |
| $t_{p(R\text{-}F)}$ | Propagation delay time, $\overline{R}\uparrow$ to $\overline{FF}$ high | 2, 6, 12 | | 25 | | 45 | ns |
| $t_{p(RS\text{-}F)}$ | Propagation delay time, $\overline{RS}\downarrow$ to $\overline{FF}$ high | 7 | | 35 | | 65 | ns |
| $t_{p(RS\text{-}HF)}$ | Propagation delay time, $\overline{RS}\downarrow$ to $\overline{XO/HF}$ high | 7 | | 35 | | 65 | ns |
| $t_{p(W\text{-}E)}$ | Propagation delay time, $\overline{W}\uparrow$ to $\overline{EF}$ high | 3, 5, 11 | | 25 | | 45 | ns |
| $t_{p(R\text{-}E)}$ | Propagation delay time, $\overline{R}\downarrow$ to $\overline{EF}$ low | 3 | | 25 | | 45 | ns |
| $t_{p(RS\text{-}E)}$ | Propagation delay time, $\overline{RS}\downarrow$ to $\overline{EF}$ low | 7 | | 35 | | 65 | ns |
| $t_{p(W\text{-}HF)}$ | Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO/HF}$ low | 8 | | 35 | | 65 | ns |
| $t_{p(R\text{-}HF)}$ | Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO/HF}$ high | 8 | | 35 | | 65 | ns |
| $t_{p(R\text{-}XOL)}$ | Propagation delay time, $\overline{R}\downarrow$ to $\overline{XO/HF}$ low | 9 | | 25 | | 50 | ns |
| $t_{p(W\text{-}XOL)}$ | Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO/HF}$ low | 9 | | 25 | | 50 | ns |
| $t_{p(R\text{-}XOH)}$ | Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO/HF}$ high | 9 | | 25 | | 50 | ns |
| $t_{p(W\text{-}XOH)}$ | Propagation delay time, $\overline{W}\uparrow$ to $\overline{XO/HF}$ high | 9 | | 25 | | 50 | ns |
| $t_{p(RT\text{-}FL)}$ | Propagation delay time, $\overline{FL/RT}\downarrow$ to $\overline{HF}$, $\overline{EF}$, $\overline{FF}$ valid | 4 | | 35 | | 65 | ns |

† These values are characterized but not currently tested.
‡ Only applies when data is automatically read (see Figure 5)

## PARAMETER MEASUREMENT INFORMATION

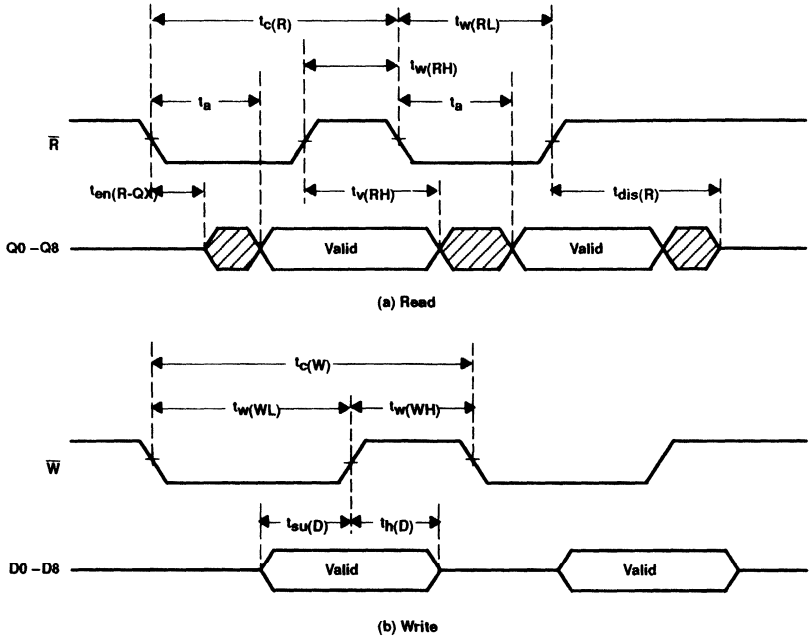



**Figure 1. Asynchronous Waveforms**

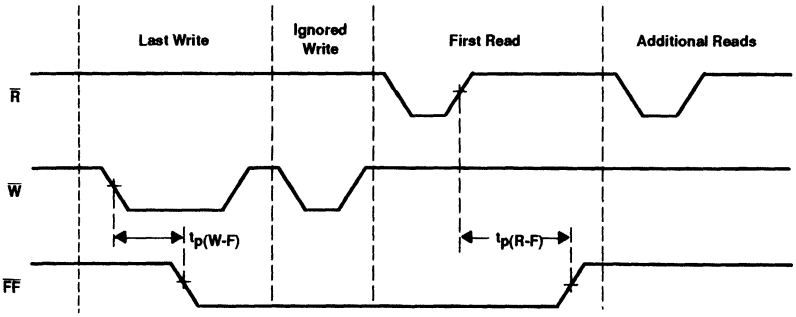



**Figure 2. Full Flag Waveforms**

## PARAMETER MEASUREMENT INFORMATION

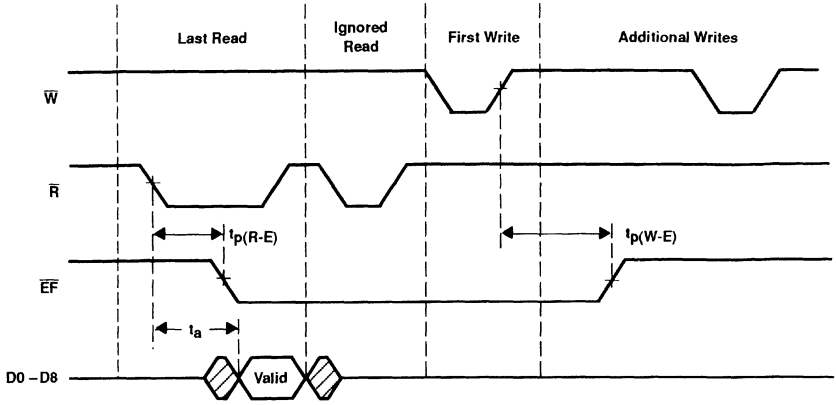



Figure 3. Empty Flag Waveforms

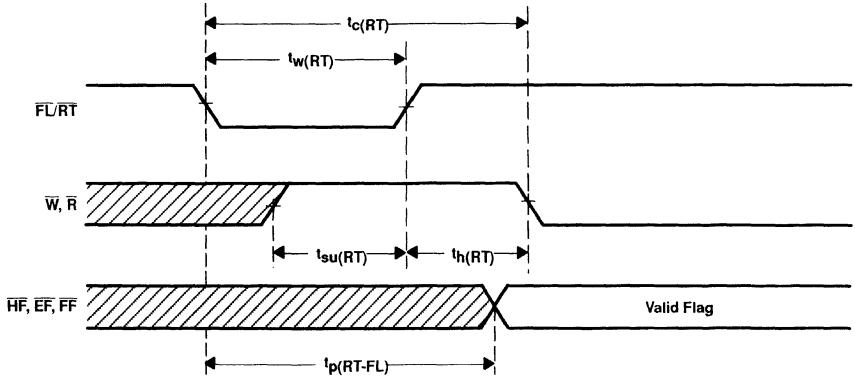



Figure 4. Retransmit Waveforms (see Note 2)

NOTE 2: The $\overline{EF}$, $\overline{FF}$, and $\overline{XO}/\overline{HF}$ status flags will be valid after completion of the retransmit cycle.

## PARAMETER MEASUREMENT INFORMATION

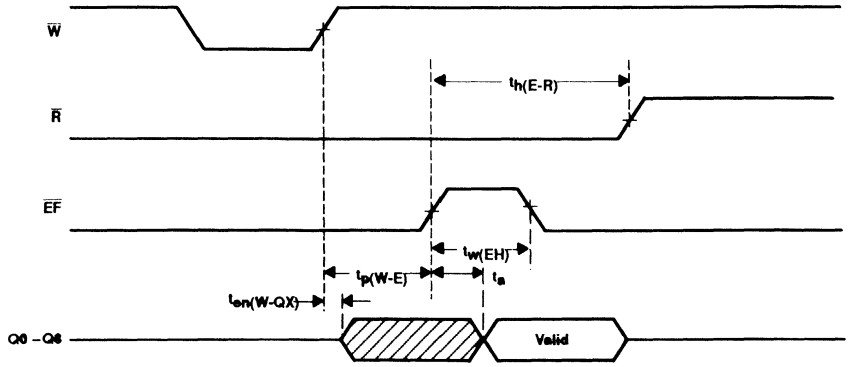



Figure 5. Automatic Read Waveforms

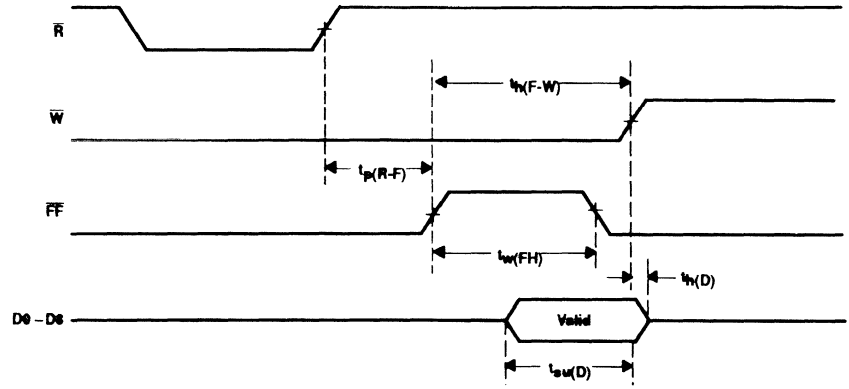



Figure 6. Automatic Write Waveforms

## PARAMETER MEASUREMENT INFORMATION

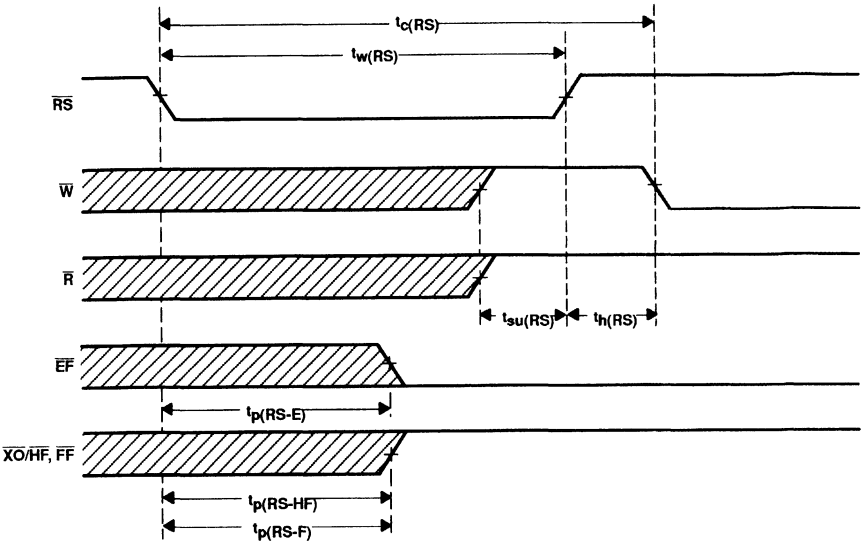



Figure 7. Master Reset Waveforms

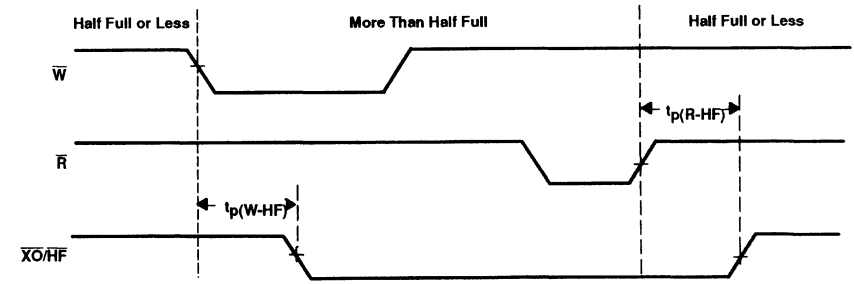



Figure 8. Half-Full Flag Waveforms

## PARAMETER MEASUREMENT INFORMATION

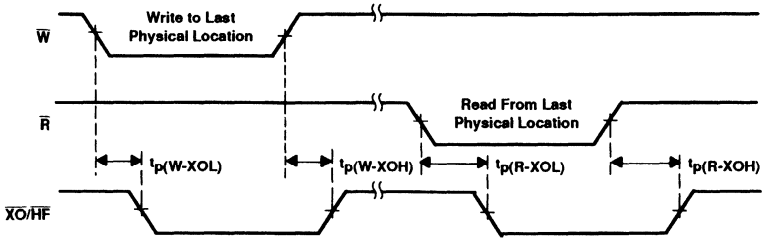



Figure 9. Expansion-Out Waveforms

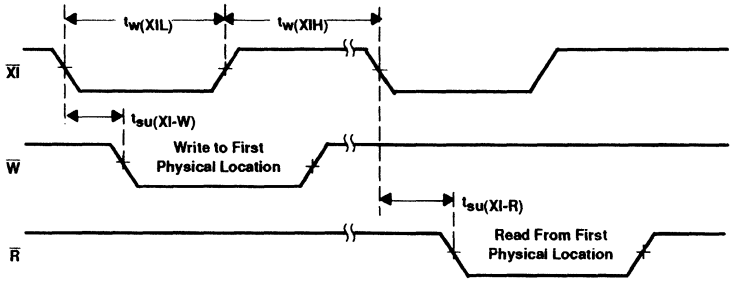



Figure 10. Expansion-In Waveforms

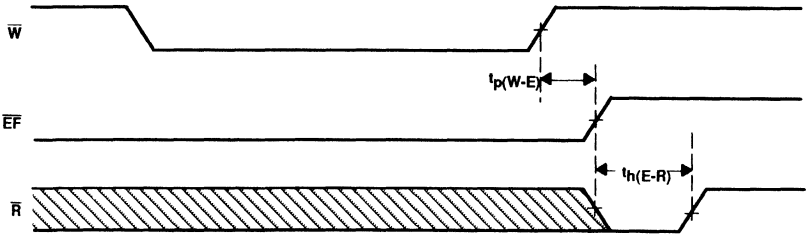



Figure 11. Minimum Timing for an Empty Flag Coincident Read Pulse

## PARAMETER MEASUREMENT INFORMATION

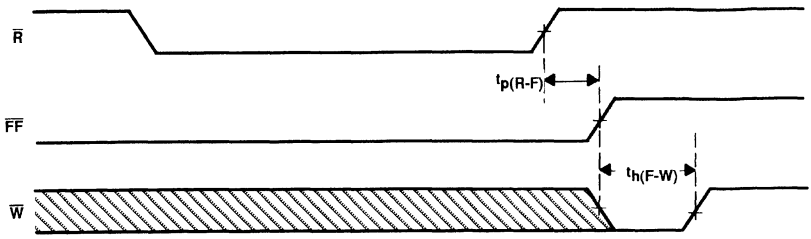



**Figure 12. Minimum Timing for a Full Flag Coincident Write Pulse**

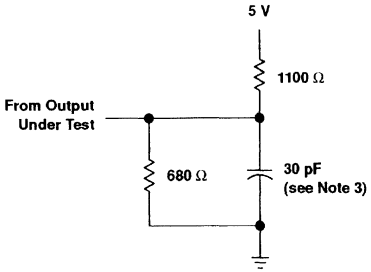



**Figure 13. Load Circuit**

NOTE 3: Includes probe and jig capacitance

## PARAMETER MEASUREMENT INFORMATION

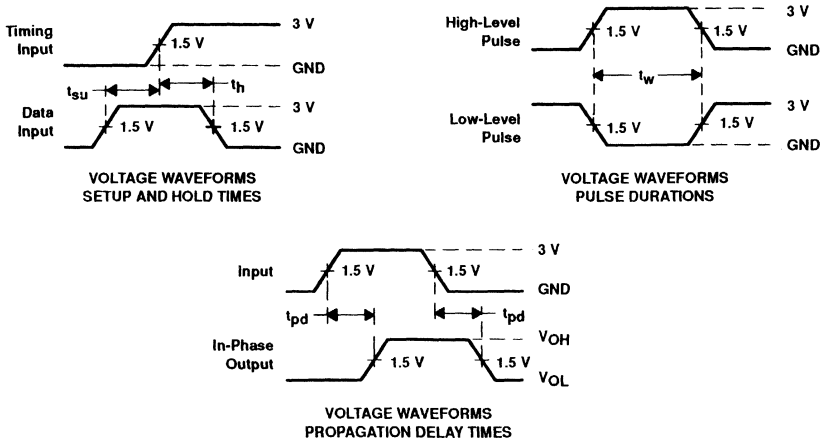



Figure 14. Timing Reference Levels

## APPLICATION INFORMATION

Combining two or more devices to create one FIFO with a greater number of memory bits is accomplished in two different ways. Width expansion increases the number of bits in each word by connecting FIFOs with the same depth in parallel. Depth expansion uses the built-in expansion logic to daisy-chain two or more devices for applications requiring more than 2048 or 4096 words of storage. Width expansion and depth expansion can be used together.

### width expansion

Word-width expansion is achieved by connecting the corresponding input control to multiple devices with the same depth. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be monitored from any one device. Figure 15 shows two FIFOs in a width-expansion configuration. Note that both devices have their expansion in ($\overline{XI}$) inputs tied to ground. This disables the depth-expansion function of the device, allowing the first load/retransmit ($\overline{FL}/\overline{RT}$) input to function as a retransmit ($\overline{RT}$) input and the expansion out/half-full ($\overline{XO}/\overline{HF}$) output to function as a half-full ($\overline{HF}$) flag.

### depth expansion

The SN74ACT7203L/7204L is easily expanded in depth. Figure 16 shows the connections used to depth expand three SN74ACT7203L/7204L devices. Any depth can be attained by adding additional devices to the chain. The SN74ACT7203L/7204L operates in depth expansion under the following conditions (see Figure 16):

1. The first device in the chain is designated by tying the first load ($\overline{FL}$) input to ground.
2. All other devices must have their $\overline{FL}$ inputs at a high logic level.
3. The expansion out ($\overline{XO}$) output of each device must be tied to the expansion in ($\overline{XI}$) input of the next device.
4. External logic is needed to generate a composite full flag ($\overline{FF}$) and empty flag ($\overline{EF}$) (all $\overline{FF}$ outputs must be ORed together, and all $\overline{EF}$ outputs must be ORed together).
5. The retransmit ($\overline{RT}$) and half-full ($\overline{HF}$) functions are not available in the depth-expanded configuration.

### combined depth and width expansion

Both expansion techniques can be used together to increase depth and width. This is done by first creating depth-expanded units and then connecting them in a width-expanded configuration (see Figure 17).

## APPLICATION INFORMATION

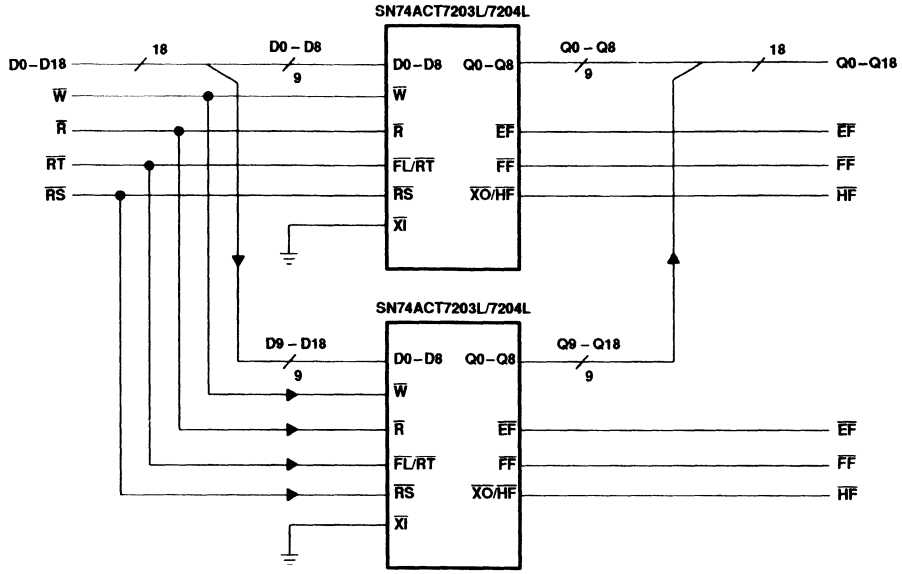



Figure 15. Word-Width Expansion: 2048/4096-Word By 18-Bit

## APPLICATION INFORMATION

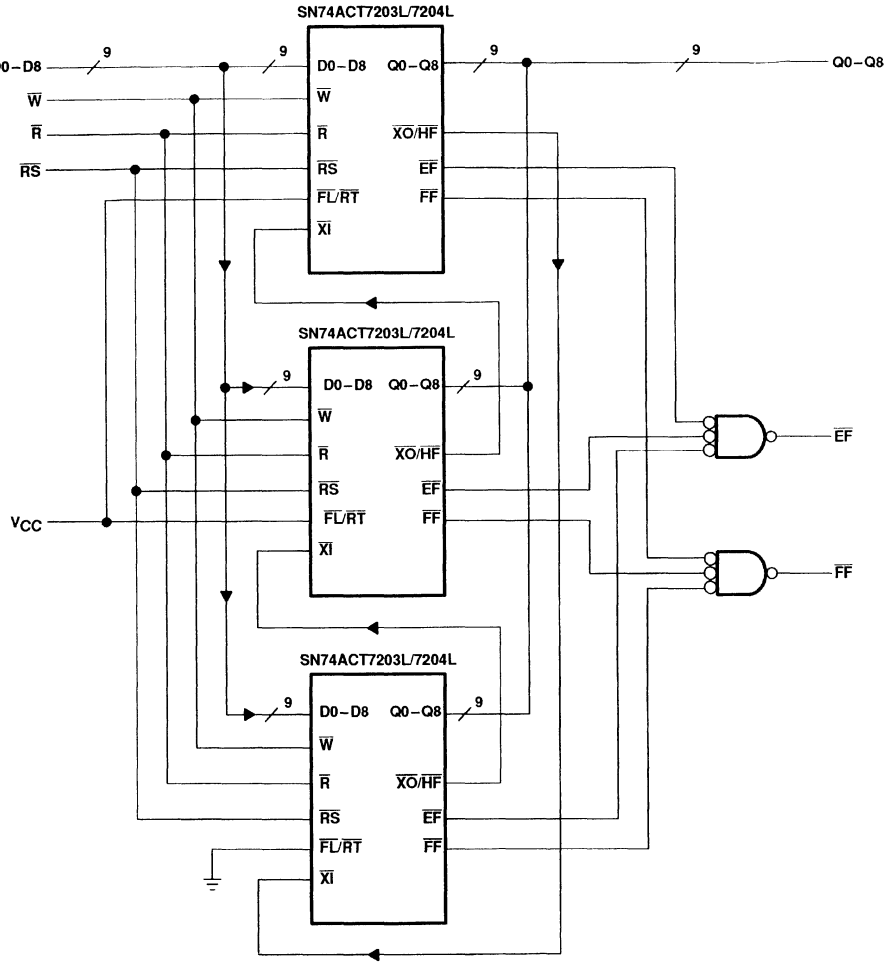



Figure 16. Word-Depth Expansion: 6144 × 9/12288 × 9 FIFO Memory



TEXAS INSTRUMENTS

## APPLICATION INFORMATION

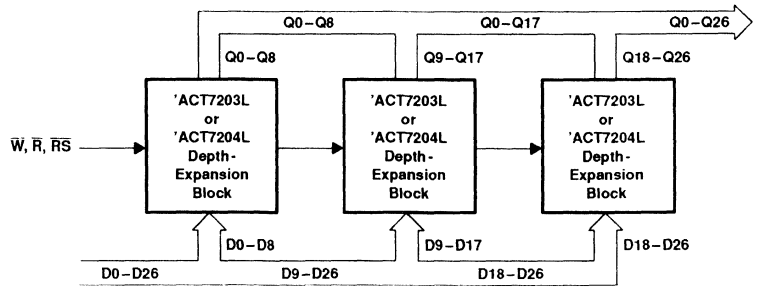
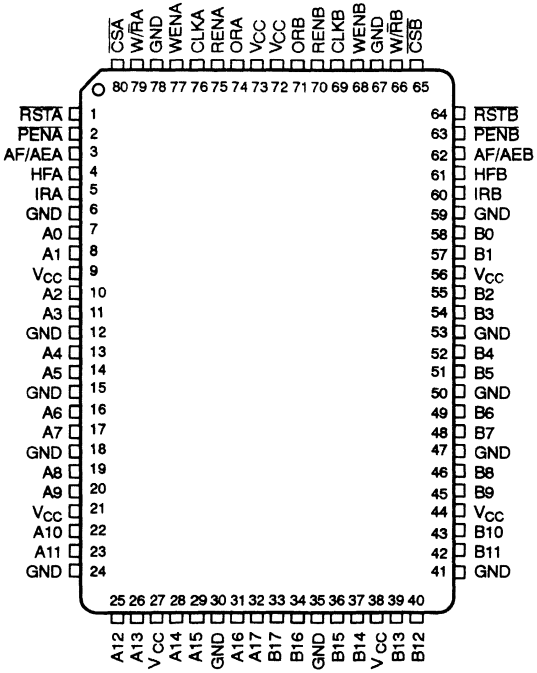



Figure 17. Word-Depth Plus Word-Width Expansion

SCBS125A–D4502, JULY 1992–REVISED AUGUST 1992

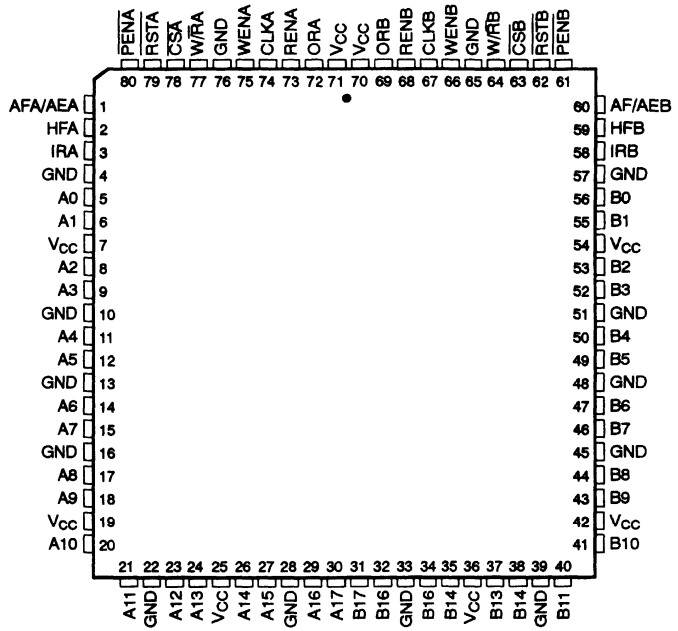
- Member of the Texas Instruments *Widebus* ™ Family
- Free-Running CLKA and CLKB May be Asynchronous or Coincident
- Read and Write Operations Synchronized to Independent System Clocks
- Two Separate 512 × 18 Clocked FIFOs Buffering Data in Opposite Directions
- IRA and ORA Synchronized to CLKA
- IRB and ORB Synchronized to CLKB
- Microprocessor Interface Control Logic
- Programmable Almost Full/Almost Empty Flags
- Fast Access Times of 9 ns With a 50-pF Load and Simultaneous Switching Data Outputs
- Data Rates up to 80 MHz
- Advanced BICMOS Technology
- Available in 80-pin Quad Flatpack (PH) and Space-Saving 80-pin Shrink Quad Flatpack (PN)

**PH OR PN PACKAGE**
**(TOP VIEW)**




Widebus is a trademark of Texas Instruments Incorporated.

**PN PACKAGE**
**(TOP VIEW)**




## description

A FIFO memory is a storage device that allows data to be read from its array in the same order it is written. The SN74ABT7819 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. Two independent 512 × 18 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions, a half-full flag, and a programmable almost full/almost empty flag.

The SN74ABT7819 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The state of the A0–A17 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The A0–A17 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to FIFOA–B from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, WENA is high, and the IRA flag is high. Data is read from FIFOB–A to the A0–A17 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, RENA is high, and the ORA flag is high.

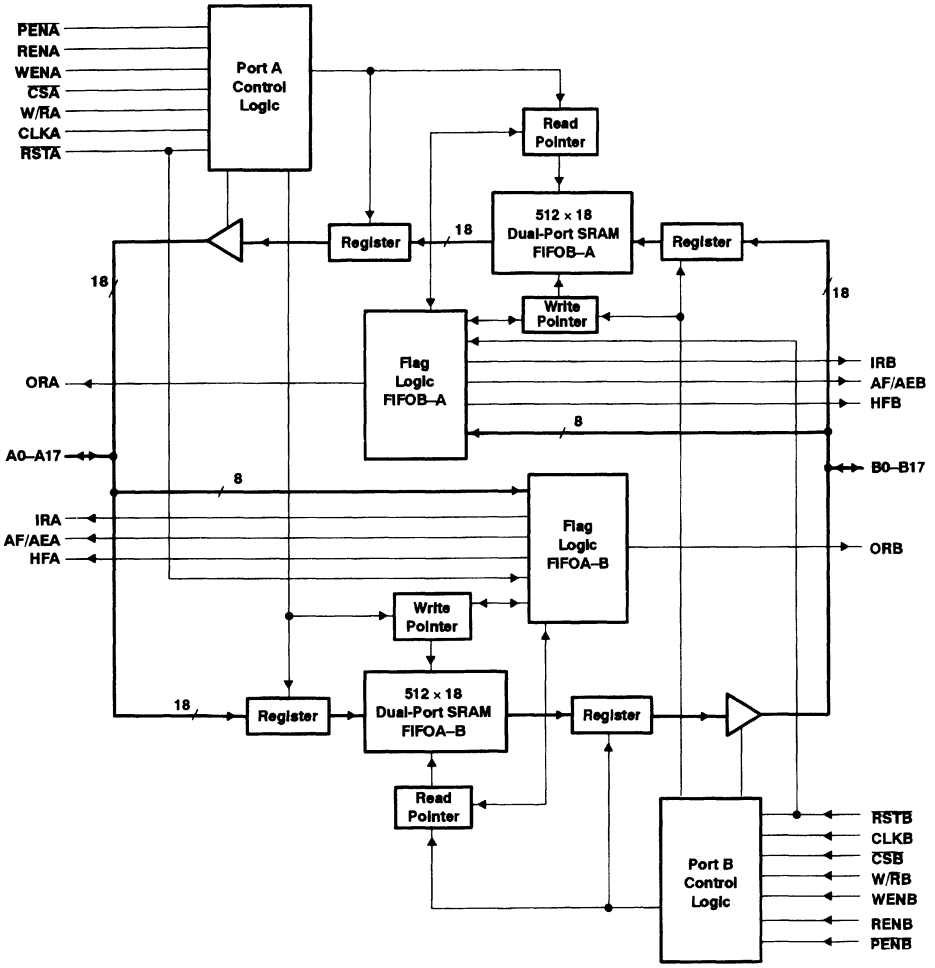
**description (continued)**

The state of the B0–B17 outputs is controlled by $\overline{CSB}$ and W/$\overline{RB}$. When both $\overline{CSB}$ and W/$\overline{RB}$ are low, the outputs are active. The B0–B17 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. Data is written to FIFOB–A from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is high, WENB is high, and the IRB flag is high. Data is read from FIFOB–A to the B0–B17 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, RENB is high, and the ORB flag is high.

The setup and hold time constraints for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are for enabling write and read operations on memory and are not related to the high-impedance control of the data outputs. If a port's read enable (RENA or RENB) and write enable (WENA or WENB) are set low during a clock cycle, the chip select and write/read select may switch at any time during the cycle to change the state of the data outputs.

The input ready and output ready flags of a FIFO are two-stage synchronized to the port clocks for use as reliable control signals. CLKA synchronizes the status of the input ready flag of FIFOA–B (IRA) and the output ready flag of FIFOB–A (ORA). CLKB synchronized the status of the input ready flag of FIFOB–A (IRB) and the output ready flag of FIFOA–B (ORB). When the input ready flag of a port is low, the FIFO receiving input from the port is full, and writes are disabled to its array. When the output ready flag of a port is low, the FIFO that outputs data to the port is empty, and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO's output register at the same time its output ready flag is asserted (high). When the memory is read empty and the output ready flag is forced low, the last valid data remains on the FIFO outputs until the output ready flag is asserted (high) again. In this way, a high on the output ready flag indicates new data is present on the FIFO outputs.

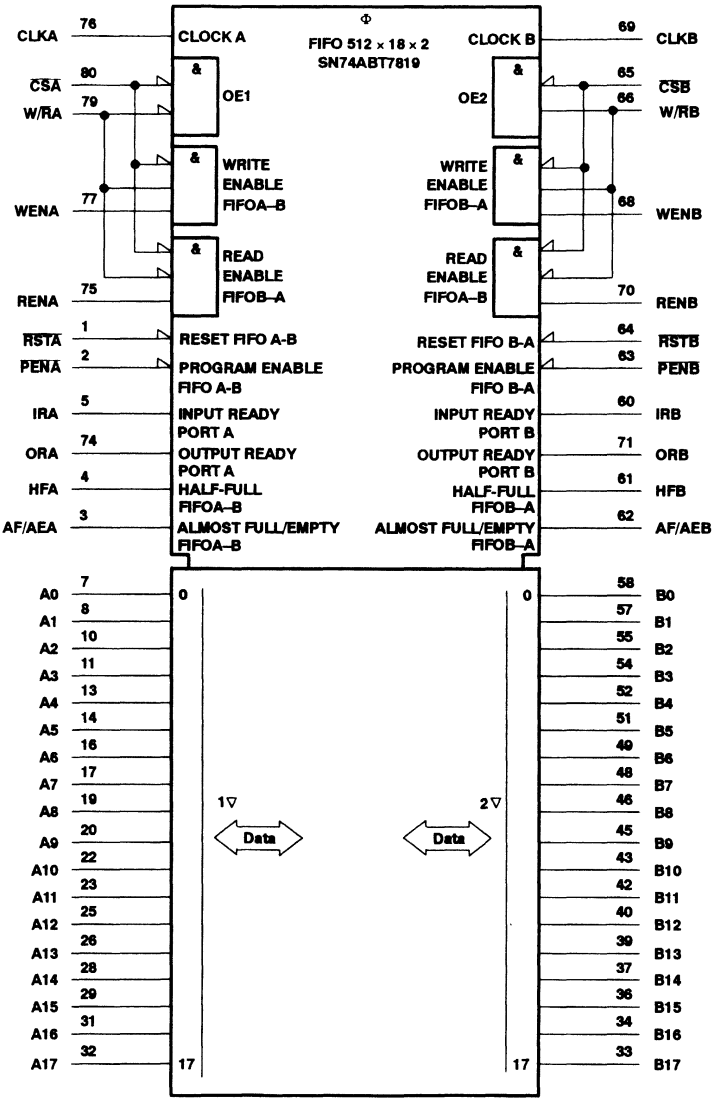
## functional block diagram





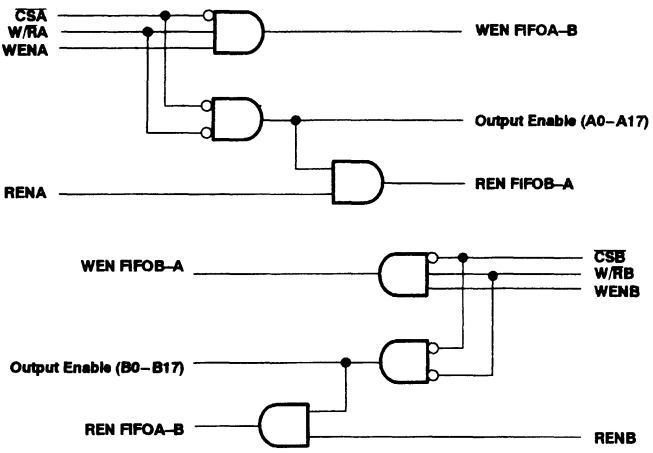

TEXAS INSTRUMENTS

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the PH package.

## enable logic diagram (positive logic)




**FUNCTION TABLES**

| SELECT INPUTS | | | | | A0–A17 | A Port Operation |
|---|---|---|---|---|---|---|
| CLKA | $\overline{CSA}$ | W/$\overline{RA}$ | WENA | RENA | | |
| X | H | X | X | X | High Z | None |
| ↑ | L | H | H | X | High Z | Write A0–A17 to FIFOA–B |
| ↑ | L | L | X | H | Active | Read FIFOB–A to A0–A17 |

| SELECT INPUTS | | | | | B0–B17 | B Port Operation |
|---|---|---|---|---|---|---|
| CLKB | $\overline{CSB}$ | W/$\overline{RB}$ | WENB | RENB | | |
| X | H | X | X | X | High Z | None |
| ↑ | L | H | H | X | High Z | Write B0–B17 to FIFOB–A |
| ↑ | L | L | X | H | Active | Read FIFOA–B to B0–B17 |

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A17 | I/O | Port A data. 18-bit bidirectional data port for side A |
| AF/AEA | O | FIFOA–B almost full/almost empty flag. Depth offsets may be programmed for this flag, or the default value of 128 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AEA is high when X or less words or (512 minus Y) or more words are stored in FIFOA–B. AF/AEA is forced high when FIFOA–B is reset. |
| AF/AEB | O | FIFOB–A almost full/almost empty flag. Depth offsets may be programmed for this flag, or the default value of 128 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AEB is high when X or less words or (512 minus Y) or more words are stored in FIFOB–A. AF/AEB is forced high when FIFOB–A is reset. |
| B0–B17 | I/O | Port B data. 18-bit bidirectional data port for side B |
| CLKA | I | Port A clock. CLKA is a continuous clock that synchronizes all data transfers through port A to its low-to-high transition and may be asynchronous or coincident to CLKB. |
| CLKB | I | Port B clock. CLKB is a continuous clock that synchronizes all data transfers through port B to its low-to-high transition and may be asynchronous or coincident to CLKA. |
| $\overline{CSA}$ | I | Port A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to either write data from A0–A17 to FIFOA–B or read data from FIFOB–A to A0–A17. The A0–A17 outputs are in the high-impedance state when $\overline{CSA}$ is high. |
| $\overline{CSB}$ | I | Port B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to either write data from B0–B17 to FIFOB–A or read data from FIFOA–B to B0–B17. The B0–B17 outputs are in the high-impedance state when $\overline{CSB}$ is high. |
| HFA | O | FIFOA–B half-full flag. HFA is high when FIFOA–B contains 256 or more words and is low when FIFOA–B contains 255 or less words. HFA is set low after FIFOA–B is reset. |
| HFB | O | FIFOB–A half-full flag. HFB is high when FIFOB–A contains 256 or more words and is low when FIFOB–A contains 255 or less words. HFB is set low after FIFOB–A is reset. |
| IRA | O | Port A input ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFOA–B is full, and writes to its array are disabled. IRA is set low during a FIFOA–B reset and is set high on the second low-to-high transition of CLKA after reset. |
| IRB | O | Port B input ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFOB–A is full, and writes to its array are disabled. IRB is set low during a FIFOB–A reset and is set high on the second low-to-high transition of CLKB after reset. |
| ORA | O | Port A output ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFOB–A is empty, and reads from its array are disabled. The last valid word remains on the FIFOB–A outputs when ORA is low. Ready data is present for the A0–A17 outputs when ORA is high. ORA is set low during a FIFOB–A reset and goes high on the third low-to-high transition of CLKA after the first word is loaded to an empty FIFOB–A. |
| ORB | O | Port B output ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFOA–B is empty, and reads from its array are disabled. The last valid word remains on the FIFOA–B outputs when ORB is low. Ready data is present for the B0–B17 outputs when ORB is high. ORB is set low during a FIFOA–B reset and goes high on the third low-to-high transition of CLKB after the first word is loaded to an empty FIFOA–B. |
| $\overline{PENA}$ | I | AF/AEA program enable. After FIFOA–B is reset and before a word is written to its array, the binary value on A0–A7 is latched as an AF/AEA offset when $\overline{PENA}$ is low and CLKA is high. |
| $\overline{PENB}$ | I | AF/AEB program enable. After FIFOB–A is reset and before a word is written to its array, the binary value on B0–B7 is latched as an AF/AEB offset when $\overline{PENB}$ is low and CLKB is high. |
| RENA | I | Port A read enable. A high level on RENA enables data to be read from FIFOB–A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is low, and ORA is high. |
| RENB | I | Port B read enable. A high level on RENB enables data to be read from FIFOA–B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{R}$B is low, and ORB is high. |
| $\overline{RSTA}$ | I | FIFOA–B reset. To reset FIFOA–B, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RSTA}$ is low. This sets HFA low, IRA low, ORB low, and AF/AEA high. |
| $\overline{RSTB}$ | I | FIFOB–A reset. To reset FIFOB–A, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RSTB}$ is low. This sets HFB low, IRB low, ORA low, and AF/AEB high. |
| WENA | I | Port A write enable. A high level on WENA enables data on A0–A17 to be written into FIFOA–B on the low-to-high transition of CLKA when W/$\overline{R}$A is high, $\overline{CSA}$ is low, and IRA is high. |

**Terminal Functions (continued)**

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| WENB | I | Port B write enable. A high level on WENB enables data on B0–B17 to be written into FIFOB–A on the low-to-high transition of CLKB when W/$\overline{R}$B is high, $\overline{CSB}$ is low, and IRB is high. |
| W/$\overline{R}$A | I | Port A write/$\overline{read}$ select. A high on W/$\overline{R}$A enables A0–A17 data to be written to FIFOA–B on a low-to-high transition of CLKA when WENA is high, $\overline{CSA}$ is low, and IRA is high. A low on W/$\overline{R}$A enables data to be read from FIFOB–A on a low-to-high transition of CLKA when RENA is high, $\overline{CSA}$ is low, and ORA is high. The A0–A17 outputs are in the high-impedance state when W/$\overline{R}$A is high. |
| W/$\overline{R}$B | I | Port B write/$\overline{read}$ select. A high on W/$\overline{R}$B enables B0–B17 data to be written to FIFOB–A on a low-to-high transition of CLKB when WENB is high, $\overline{CSB}$ is low, and IRB is high. A low on W/$\overline{R}$B enables data to be read from FIFOA–B on a low-to-high transition of CLKB when RENB is high, $\overline{CSB}$ is low, and ORB is high. The B0–B17 outputs are in the high-impedance state when W/$\overline{R}$B is high. |

## timing diagrams

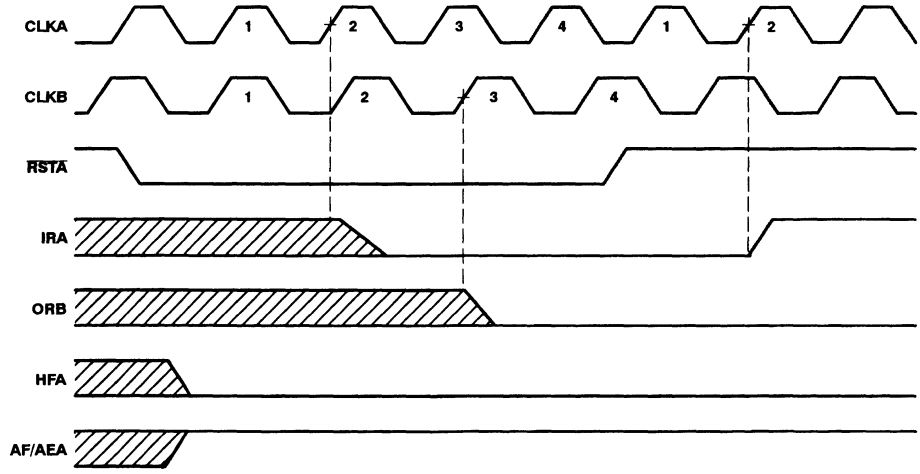
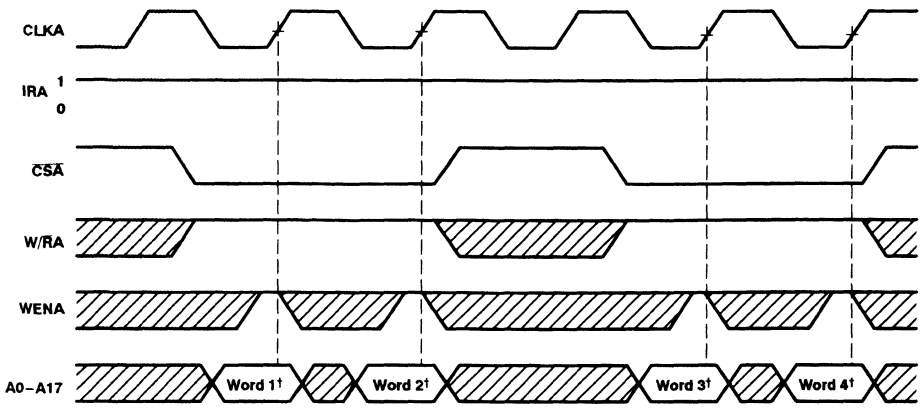


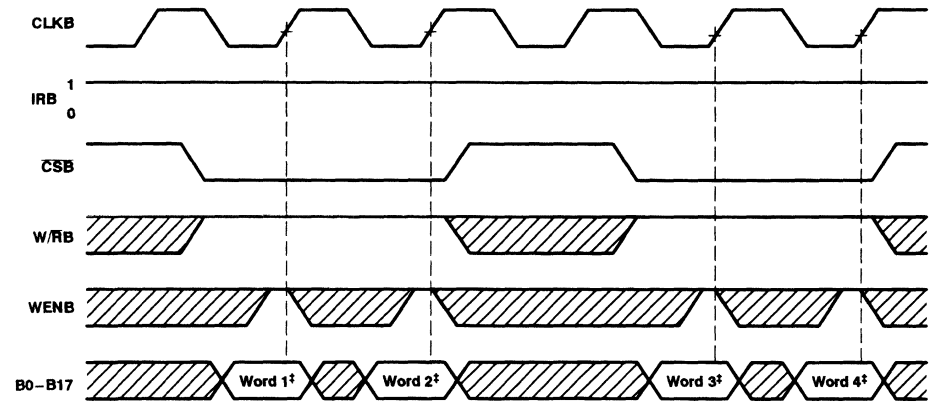

**Figure 1. Reset Cycle For FIFOA–B†**

† FIFOB–A is reset in the same manner.




† Written to FIFOA–B

**Figure 2. Write Timing – Port A**




‡ Written to FIFOB–A

**Figure 3. Write Timing – Port B**

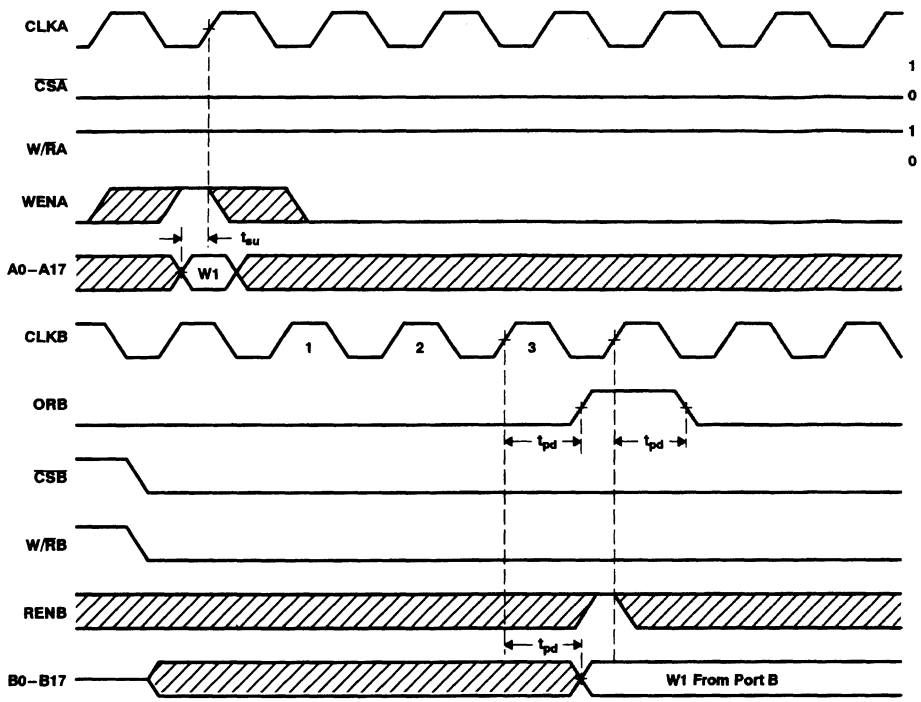



**Figure 4. ORB Flag Timing and First Data Word Fallthrough When FIFOA–B Is Empty†**

† Operation of FIFOB–A is identical to that of FIFOA–B

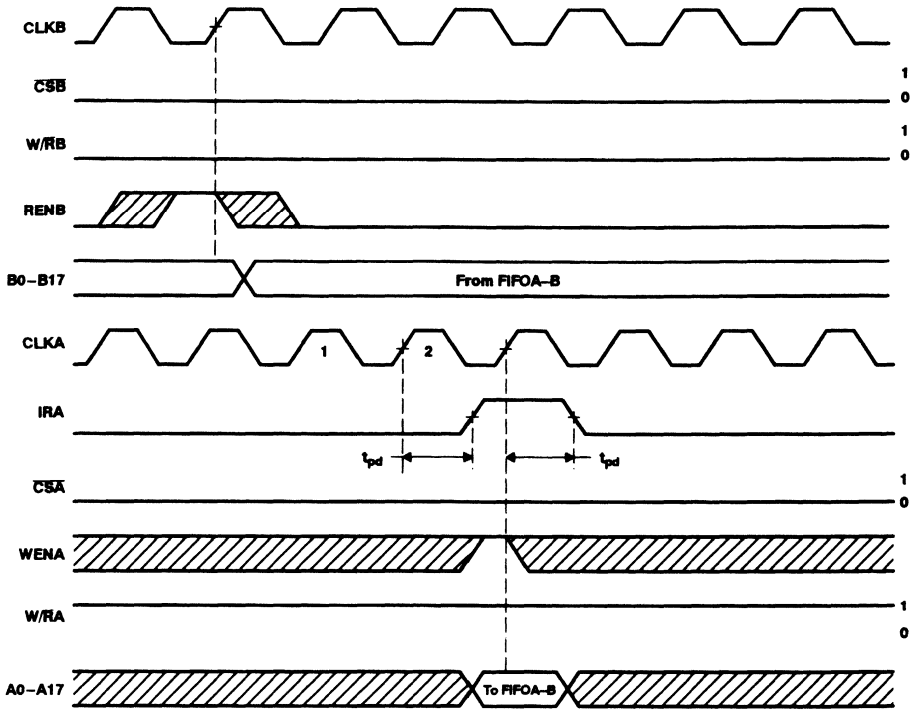
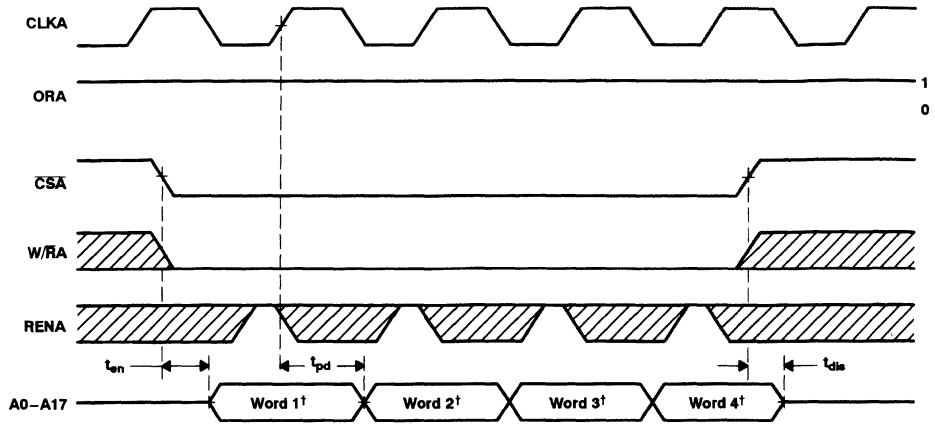



**Figure 5. Write Cycle and IRA Flag Timing When FIFOA–B is Full†**

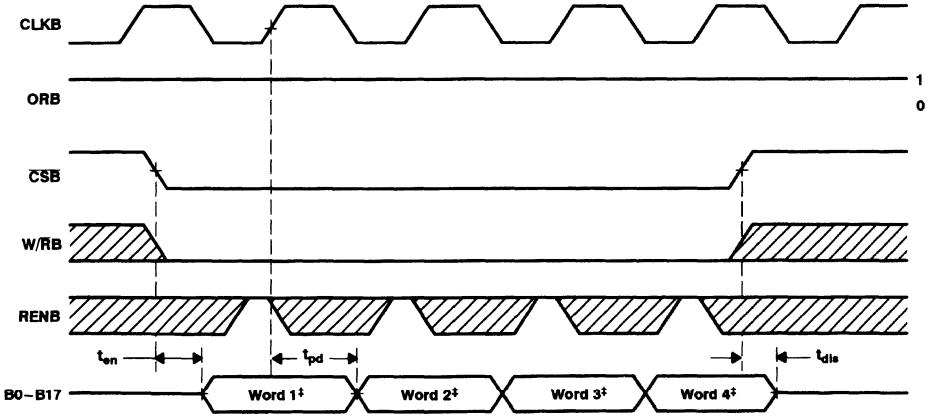
† Operation of FIFOB–A is identical to that of FIFOA–B

## read timing diagrams




† Read from FIFOB–A

**Figure 6. Read Timing – Port A**




‡ Read from FIFOA–B

**Figure 7. Read Timing – Port B**

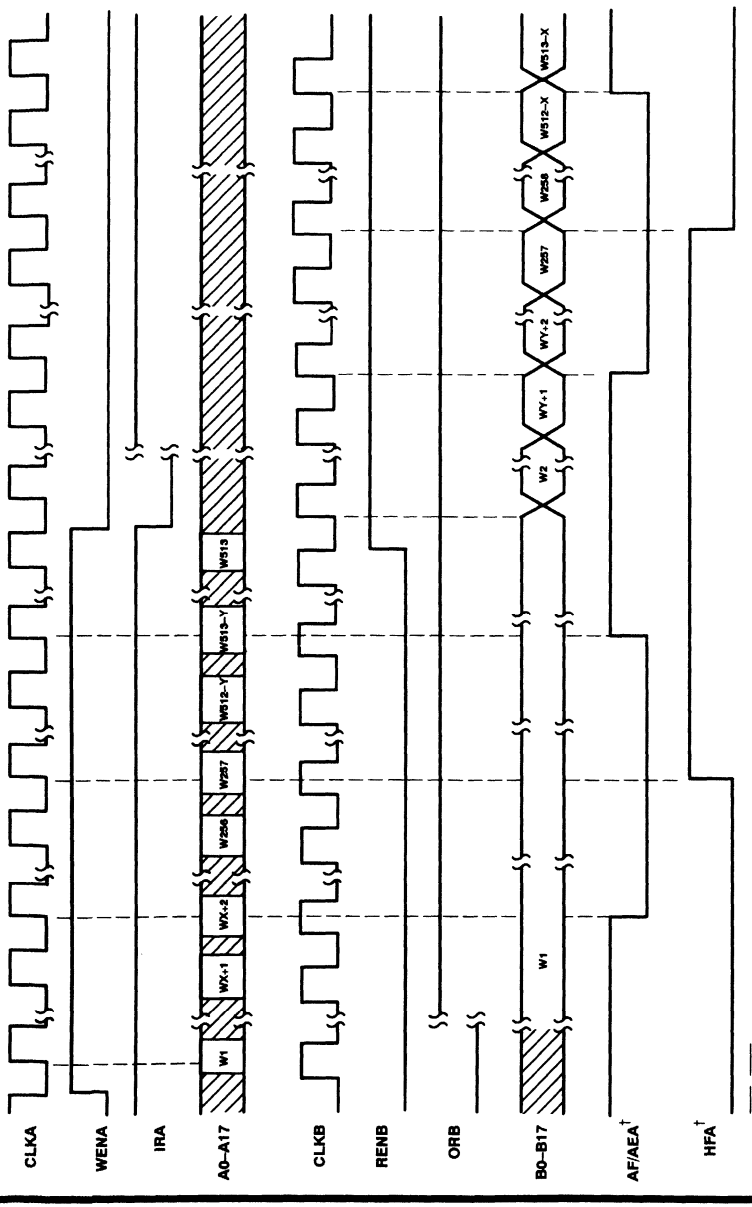



**Figure 8. FIFOA-B (HFA, AF/AEA) Asynchronous Flag Timing**

### offset values for AF/AE

The almost full/almost empty flag of each FIFO has two programmable limits, the almost empty offset value (X) and the almost full offset value (Y). They may be programmed from the input of the FIFO after it is reset and before a word is written to its memory. An AF/AE flag will be high when its FIFO contains X or less words or (512 minus Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ may be brought low after FIFOA–B is reset and only when CLKA is low. On the following low-to-high transition of CLKA, the binary value on A0–A7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of CLKA will reprogram Y to the binary value on A0–A7 at the time of the second CLKA low-to-high transition.

During the first two CLKA cycles used for offset programming, $\overline{\text{PENA}}$ may be brought high only when CLKA is low. $\overline{\text{PENA}}$ may be brought high at any time after the second CLKA pulse used for offset programming returns low. A maximum value of 255 may be programmed for either X or Y. To use the default values of X = Y = 128, $\overline{\text{PENA}}$ must be tied high. No data is stored in FIFOA–B while the AF/AEA offsets are programmed.

The AF/AEB flag is programmed in the same manner with $\overline{\text{PENB}}$ enabling CLKB to program the offset values taken from B0–B7.

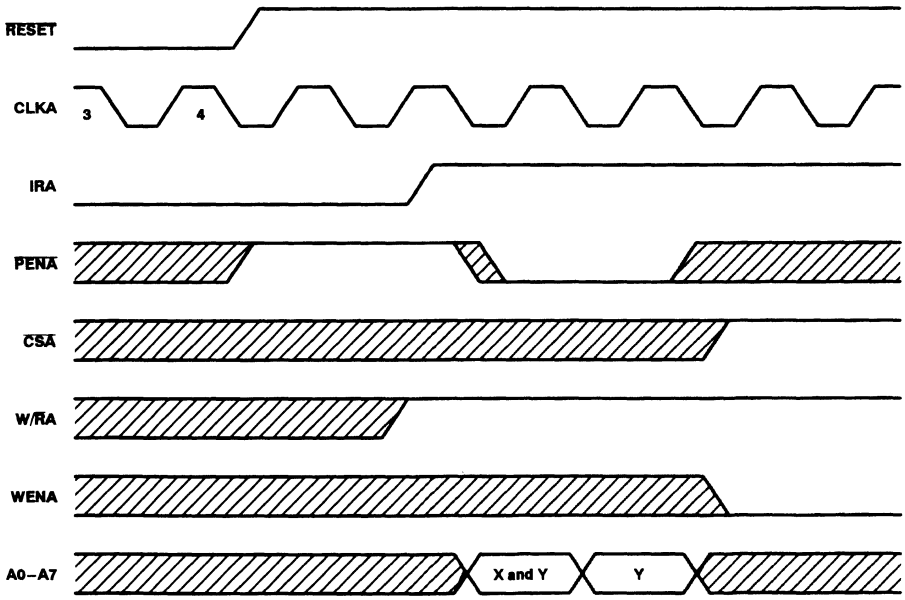



**Figure 9. Timing Diagram to Program X and Y Separately for AF/AEA**

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −0.5 V to $V_{CC}$ + 0.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$ ..... −0.5 V to 5.5 V
Current into any output in the low state, $I_O$ ..... 48 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... −18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | −12 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −3 mA | | | 2.5 | | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = −3 mA | | | 3 | | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −12 mA | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | | | 0.5 | | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | | | ±1 | µA |
| $I_{OZH}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | | 50 | µA |
| $I_{OZL}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | | −50 | µA |
| $I_O$¶ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | | | −40 | −100 | −180 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | Outputs high | | | 15 | mA |
| | | | | | Outputs low | | | 95 | |
| | | | | | Outputs disabled | | | 15 | |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | | | 6 | | pF |
| $C_o$ | Flags | $V_O$ = 2.5 V or 0.5 V | | | | | 4 | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## timing characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | | | 'ABT7819-12 | | 'ABT7819-15 | | 'ABT7819-20 | | 'ABT7819-30 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 80 | | 67 | | 50 | | 33.3 | MHz |
| $t_w$ | Pulse duration | CLKA, CLKB high or low | 4.5 | | 6 | | 8 | | 11 | | ns |
| $t_{su}$ | Setup time | A0–A17 before CLKA↑ and B0–B17 before CLKB↑ | 3 | | 4 | | 5 | | 5 | | ns |
| | | $\overline{CSA}$ before CLKA↑ and $\overline{CSB}$ before CLKB↑ | 6 | | 6 | | 7 | | 7 | | |
| | | W/$\overline{RA}$ before CLKA↑ and W/$\overline{RB}$ before CLKB↑ | 6 | | 6 | | 7 | | 7 | | |
| | | WENA before CLKA↑ and WENB before CLKB↑ | 4 | | 4 | | 5 | | 5 | | |
| | | $\overline{RENA}$ before CLKA↑ and $\overline{RENB}$ before CLKB↑ | 5 | | 5 | | 5 | | 6 | | |
| | | $\overline{PENA}$ before CLKA↑ and $\overline{PENB}$ before CLKB↑ | 3 | | 4 | | 5 | | 5 | | |
| | | $\overline{RSTA}$ or $\overline{RSTB}$ low before first CLKA↑ and CLKB↑ † | 3 | | 4 | | 5 | | 5 | | |
| $t_h$ | Hold time | A0–A17 after CLKA↑ and B0–B17 after CLKB↑ | 0 | | 0 | | 0 | | 0 | | ns |
| | | $\overline{CSA}$ after CLKA↑ and $\overline{CSB}$ after CLKB↑ | 0 | | 0 | | 0 | | 0 | | |
| | | W/$\overline{RA}$ after CLKA↑ and W/$\overline{RB}$ after CLKB↑ | 0 | | 0 | | 0 | | 0 | | |
| | | WENA after CLKA↑ and WENB after CLKB↑ | 0 | | 0 | | 0 | | 0 | | |
| | | $\overline{RENA}$ after CLKA↑ and $\overline{RENB}$ after CLKB↑ | 0 | | 0 | | 0 | | 0 | | |
| | | PENA after CLKA low and PENB after CLKB low | 2 | | 2 | | 2 | | 2 | | |
| | | $\overline{RSTA}$ or $\overline{RSTB}$ low after fourth CLKA↑ and CLKB↑ † | 3 | | 3 | | 4 | | 4 | | |

† To permit the clock pulse to be utilized for reset purposes.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 10 and 12)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ABT7819-12 | | | 'ABT7819-15 | | 'ABT7819-20 | | 'ABT7819-30 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKA or CLKB | | 80 | | | 67 | | 50 | | 33.3 | | MHz |
| $t_{pd}$ | CLKA↑ | A0–A17 | 4 | 7 | 9 | 4 | 10 | 4 | 12 | 4 | 14 | ns |
| | CLKB↑ | B0–B17 | 4 | 7 | 9 | 4 | 10 | 4 | 12 | 4 | 14 | |
| $t_{pd}$‡ | CLKA↑ | A0–A17 | | 6 | | | | | | | | ns |
| | CLKB↑ | B0–B17 | | 6 | | | | | | | | |
| $t_{pd}$ | CLKA↑ | IRA | 4 | | 9 | 4 | 10 | 4 | 12 | 4 | 14 | ns |
| | CLKB↑ | IRB | 4 | | 9 | 4 | 10 | 4 | 12 | 4 | 14 | |
| $t_{pd}$ | CLKA↑ | ORA | 3.5 | | 9 | 3.5 | 10 | 3.5 | 12 | 3.5 | 14 | ns |
| | CLKB↑ | ORA | 3.5 | | 9 | 3.5 | 10 | 3.5 | 12 | 3.5 | 14 | |
| $t_{pd}$ | CLKA↑ | AF/AEA | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | ns |
| | CLKB↑ | | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | |
| $t_{PLH}$ | $\overline{RSTA}$ | AF/AEA | 4 | | 12 | 4 | 14 | 4 | 15 | 4 | 16 | ns |
| $t_{pd}$ | CLKA↑ | AF/AEB | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | ns |
| | CLKB↑ | | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | |
| $t_{PLH}$ | $\overline{RSTB}$ | AF/AEB | 4 | | 12 | 4 | 14 | 4 | 15 | 4 | 16 | ns |
| | CLKA↑ | HFA | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | |
| $t_{PHL}$ | CLKB↑ | HFA | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | ns |
| | $\overline{RSTA}$ | | 4 | | 12 | 4 | 14 | 4 | 15 | 4 | 16 | |
| $t_{PHL}$ | CLKA↑ | HFB | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | ns |
| $t_{PLH}$ | CLKB↑ | HFB | 8 | | 17 | 8 | 17 | 8 | 18 | 8 | 20 | ns |
| $t_{PHL}$ | $\overline{RSTB}$ | | 4 | | 12 | 4 | 14 | 4 | 15 | 4 | 16 | |
| $t_{en}$ | $\overline{CSA}$ | A0–A17 | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | ns |
| | W/$\overline{RA}$ | | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | |
| $t_{en}$ | $\overline{CSB}$ | B0–B17 | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | ns |
| | W/$\overline{RB}$ | | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | |
| $t_{dis}$ | $\overline{CSA}$ | A0–A17 | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | ns |
| | W/$\overline{RA}$ | | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | |
| $t_{dis}$ | $\overline{CSB}$ | B0–B17 | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | ns |
| | W/$\overline{RB}$ | | 2.5 | | 8 | 2.5 | 9 | 2.5 | 10 | 2.5 | 11 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This parameter measured with a 30-pF load (see Figure 10).

## TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

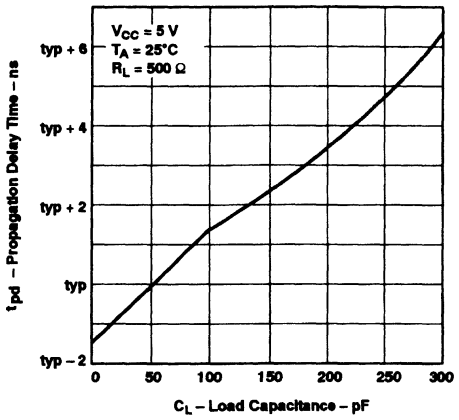



Figure 10

SUPPLY CURRENT
vs
CLOCK FREQUENCY

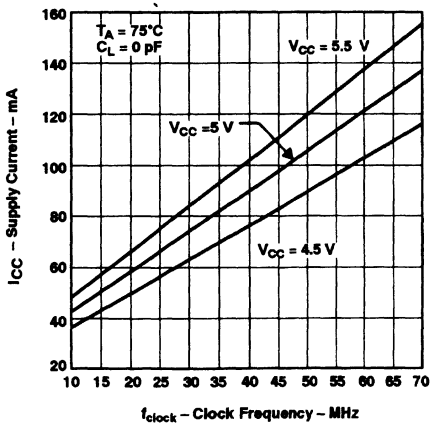



Figure 11

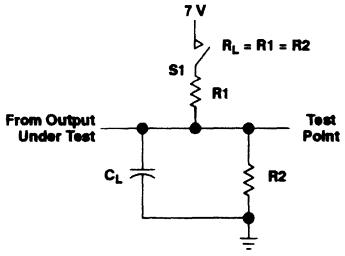
### calculating power dissipation

With $I_{CCF}$ taken from Figure 3, the maximum power dissipation based on all outputs changing states on each read may be calculated using:

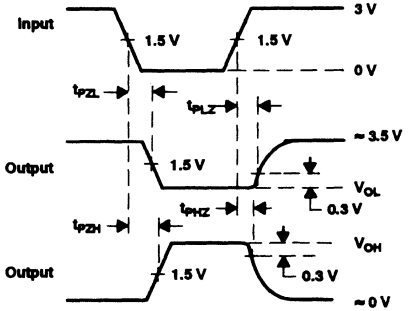
$$P_t = V_{CC} \times [I_{CCF}] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CCF}$ = maximum $I_{CC}$ per clock frequency
$C_L$ = output capacitive load
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT FOR 3-STATE OUTPUTS




VOLTAGE WAVEFORMS

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

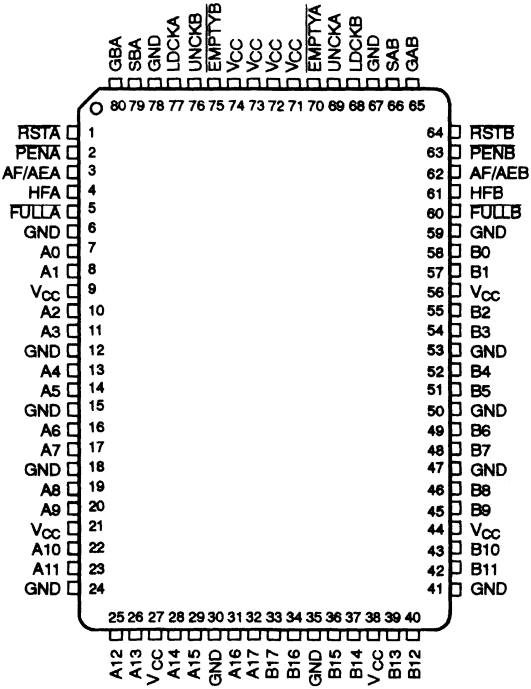
† Includes probe and test fixture capacitance.

**Figure 12. Load Circuit and Voltage Waveforms**

SCAS206A–D4503, AUGUST 1991–REVISED AUGUST 1992

- Member of the Texas Instruments *Widebus* ™ Family
- Independent Asynchronous Inputs and Outputs
- Produced in Advanced BICMOS Technology
- Two Separate 512 × 18 FIFOs Buffering Data in Opposite Directions
- Programmable Almost Full/Almost Empty Flags
- Empty, Full, and Half-Full Flags
- Fast Access Times of 12 ns With a 50-pF Load and Simultaneous Switching Data Outputs
- Supports Clock Rates Up To 67 MHz
- Available in 80-Pin Quad Flat Package (PH) and Space-Saving 80-Pin Shrink Quad Flat Package (PN)

**PH PACKAGE**
**(TOP VIEW)**

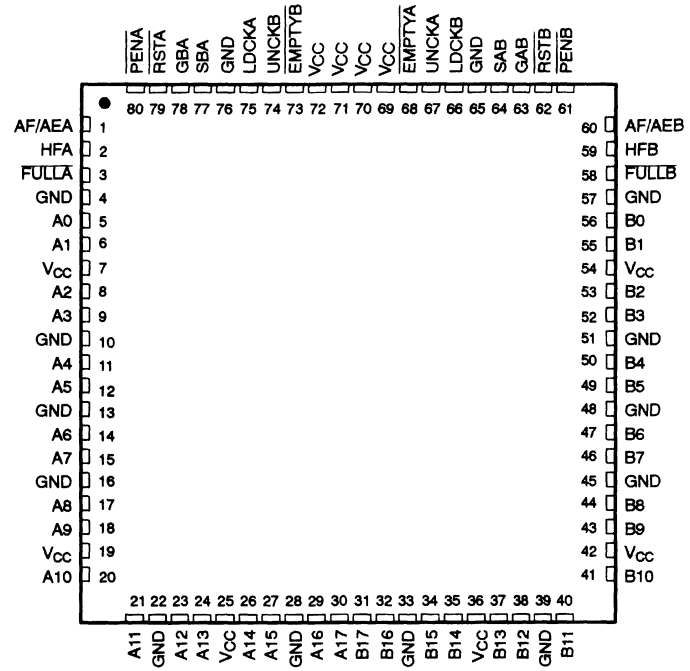



Widebus is a trademark of Texas Instruments Incorporated.



TEXAS INSTRUMENTS

PN PACKAGE
(TOP VIEW)




## description

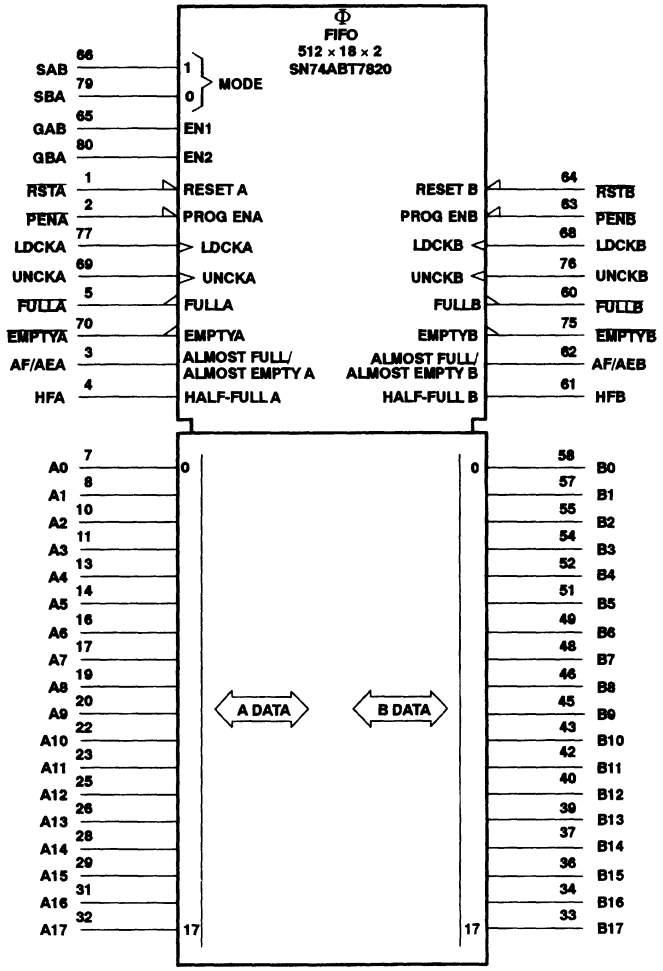
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ABT7820 is arranged as two 512 by 18-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 67 MHz with access times of 12 ns in a bit-parallel format.

The SN74ABT7820 consists of bus transceiver circuits, two 512 × 18 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable inputs GAB and GBA control the transceiver functions. The SAB and SBA control inputs select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Eight fundamental bus-management functions can be performed as shown on the operating modes page.

## Terminal Functions

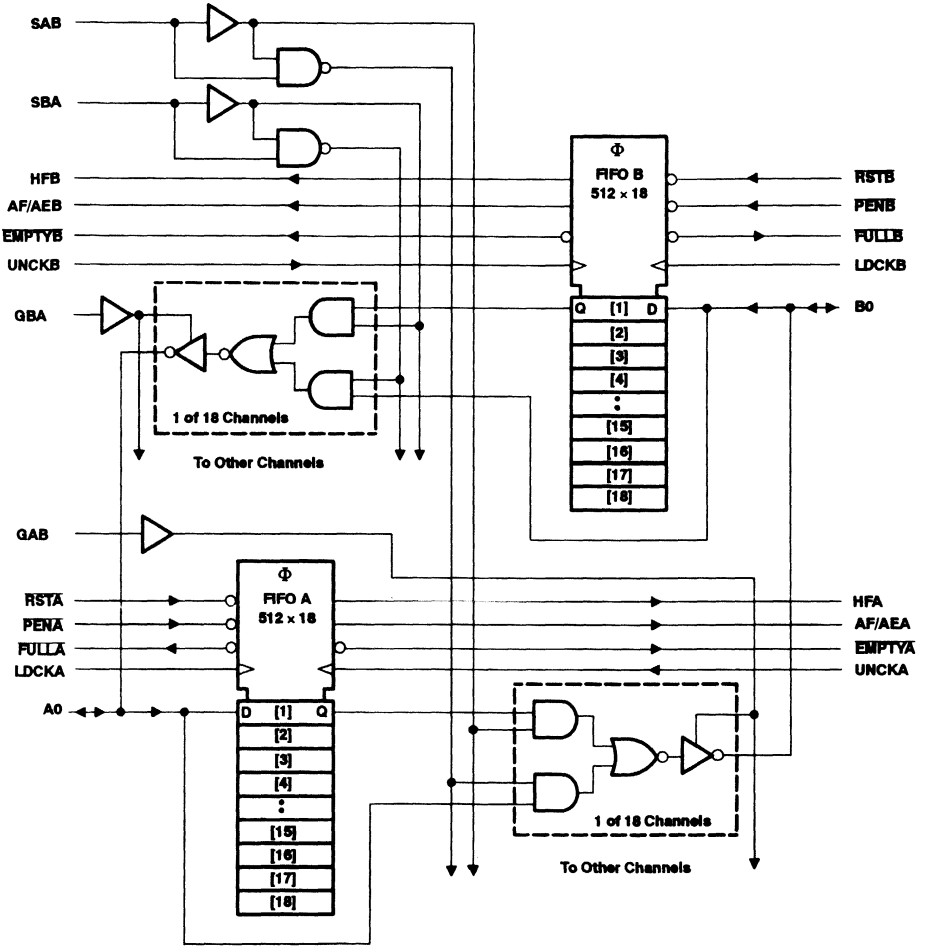
| NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A17 | I/O | Port A data. 18-bit bidirectional data port for side A. |
| AF/AEA | O | FIFO A almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 128 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AEA is high when FIFO A contains X or less words or (512 minus Y) or more words. AF/AEA is set high after FIFO A is reset. |
| AF/AEB | O | FIFO B almost full/almost empty flag. Depth offset values may be programmed for this flag, or the default value of 128 may be used for both the almost empty offset (X) and the almost full offset (Y). AF/AEB is high when FIFO B contains X or less words or (512 minus Y) or more words. AF/AEB is set high after FIFO B is reset. |
| B0–B17 | I/O | Port B data. 18-bit bidirectional data port for side B. |
| $\overline{\text{EMPTYA}}$ | O | FIFO A empty flag. $\overline{\text{EMPTYA}}$ is low when FIFO A is empty and high when FIFO A is not empty. $\overline{\text{EMPTYA}}$ is set low after FIFO A is reset. |
| $\overline{\text{EMPTYB}}$ | O | FIFO B empty flag. $\overline{\text{EMPTYB}}$ is low when FIFO B is empty and high when FIFO B is not empty. $\overline{\text{EMPTYB}}$ is set low after FIFO B is reset. |
| $\overline{\text{FULLA}}$ | O | FIFO A full flag. $\overline{\text{FULLA}}$ is low when FIFO A is full and high when FIFO A is not full. $\overline{\text{FULLA}}$ is set high after FIFO A is reset. |
| $\overline{\text{FULLB}}$ | O | FIFO B full flag. $\overline{\text{FULLB}}$ is low when FIFO B is full and high when FIFO B is not full. $\overline{\text{FULLB}}$ is set high after FIFO B is reset. |
| GAB | I | Port B output enable. B0–B17 outputs are active when GAB is high and in the high-impedance state when GAB is low. |
| GBA | I | Port A output enable. A0–A17 outputs are active when GBA is high and in the high-impedance state when GBA is low. |
| HFA | O | FIFO A half-full flag. HFA is high when FIFO A contains 256 or more words and is low when FIFO A contains 255 or less words. HFA is set low after FIFO A is reset. |
| HFB | O | FIFO B half-full flag. HFB is high when FIFO B contains 256 or more words and is low when FIFO B contains 255 or less words. HFB is set low after FIFO B is reset. |
| LDCKA | I | FIFO A load clock. Data is written into FIFO A on a low-to-high transition of LDCKA when $\overline{\text{FULLA}}$ is high. The first word written into an empty FIFO A is sent directly to the FIFO A data outputs. |
| LDCKB | I | FIFO B load clock. Data is written into FIFO B on a low-to-high transition of LDCKB when $\overline{\text{FULLB}}$ is high. The first word written into an empty FIFO B is sent directly to the FIFO B data outputs. |
| $\overline{\text{PENA}}$ | I | FIFO A program enable. After reset and before a word is written into FIFO A, the binary value on A0–A7 is latched as an AF/AEA offset value when $\overline{\text{PENA}}$ is low and LDCKA is high. |
| $\overline{\text{PENB}}$ | I | FIFO B program enable. After reset and before a word is written into FIFO B, the binary value on B0–B7 is latched as an AF/AEB offset value when $\overline{\text{PENB}}$ is low and LDCKB is high. |
| $\overline{\text{RSTA}}$ | I | FIFO A reset. A low level on $\overline{\text{RSTA}}$ resets FIFO A forcing $\overline{\text{EMPTYA}}$ low, HFA low, $\overline{\text{FULLA}}$ high, and AF/AEA high. |
| $\overline{\text{RSTB}}$ | I | FIFO B reset. A low level on $\overline{\text{RSTB}}$ resets FIFO B forcing $\overline{\text{EMPTYB}}$ low, HFB low, $\overline{\text{FULLB}}$ high, and AF/AEB high. |
| SAB | I | Port B read select. SAB selects the source of B0–B17 read data. A low level selects real-time data from A0–A17. A high level selects the FIFO A output. |
| SBA | I | Port A read select. SBA selects the source of A0–A17 read data. A low level selects real-time data from B0 – B17. A high level selects the FIFO B output. |
| UNCKA | I | FIFO A unload clock. Data is read from FIFO A on a low-to-high transition of UNCKA when $\overline{\text{EMPTYA}}$ is high. |
| UNCKB | I | FIFO B unload clock. Data is read from FIFO B on a low-to-high transition of UNCKB when $\overline{\text{EMPTYB}}$ is high. |

## logic symbol†

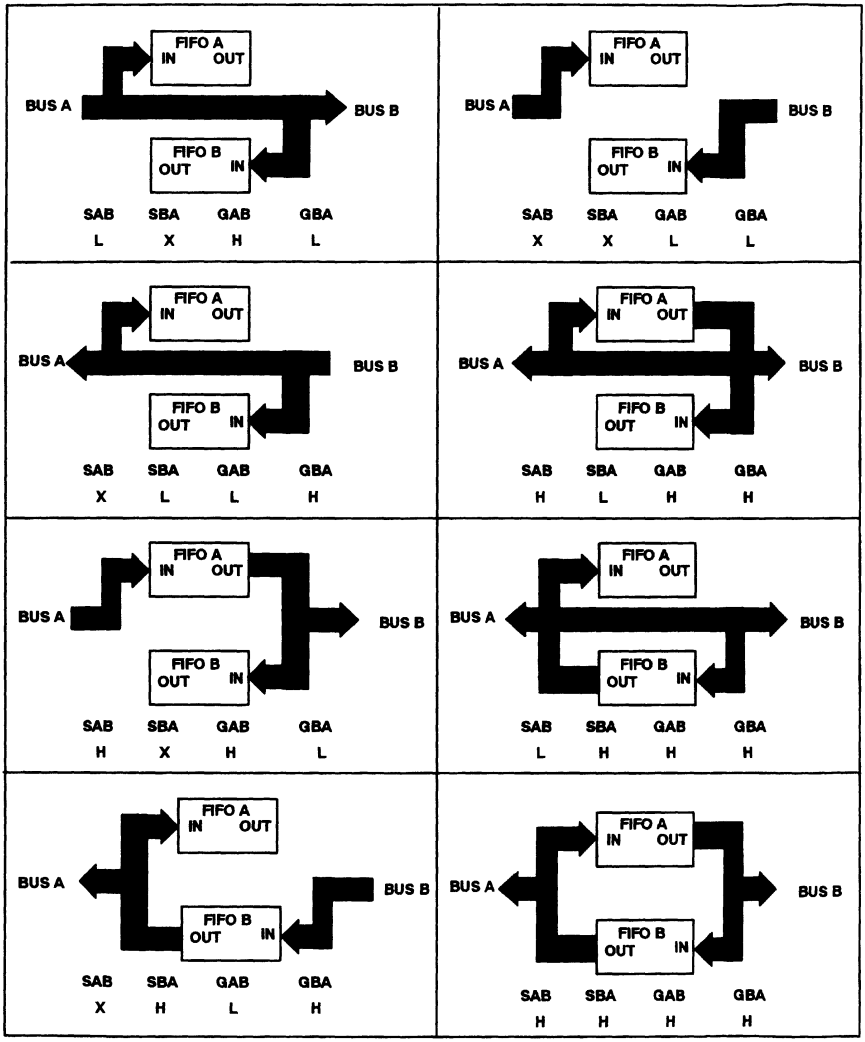



† This symbol is in accordance with ANSI/IEEE Std 91-1984.
Pin numbers shown are for the PH package.

## logic diagram (positive logic)



## operating modes






TEXAS INSTRUMENTS

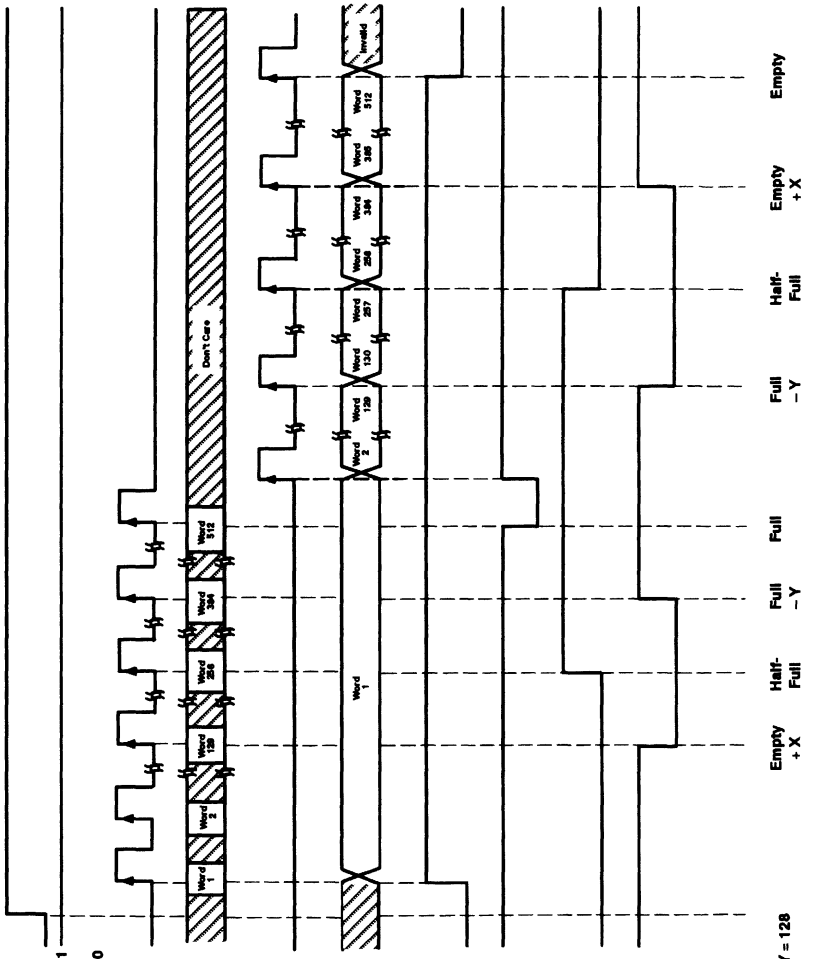
**SELECT-MODE CONTROL TABLE**

| CONTROL | | OPERATION | |
|---|---|---|---|
| SBA | SAB | A BUS | B BUS |
| L | L | Real-time B to A bus | Real-time A to B bus |
| H | L | FIFO B to A bus | Real-time A to B bus |
| L | H | Real-time B to A bus | FIFO A to B bus |
| H | H | FIFO B to A bus | FIFO A to B bus |

**OUTPUT-ENABLE CONTROL TABLE**

| CONTROL | | OPERATION | |
|---|---|---|---|
| GBA | GAB | A BUS | B BUS |
| L | L | Isolation/input to A bus | Isolation/input to B bus |
| H | L | A bus enabled | Isolation/input to B bus |
| L | H | Isolation/input to A bus | B bus enabled |
| H | H | A bus enabled | B bus enabled |

## timing diagram for FIFO A†




† SAB = GAB = H, GBA = L
Operation of FIFO B is identical to that of FIFO A

### offset values for AF/AE

The almost full/almost empty flag of each FIFO has two programmable limits: the almost empty offset value (X) and the almost full offset value (Y). The offsets of a flag may be programmed from the input of its FIFO after it is reset and before any data is written to its memory. An AF/AE flag is high when its FIFO contains X or less words or (512 minus Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ may be brought low after FIFO A is reset and only when LDCKA is low. On the following low-to-high transition of LDCKA, the binary value on A0–A7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of LDCKA will reprogram Y to the binary value on A0–A7 at the time of the second LDCKA low-to-high transition.

$\overline{\text{PENA}}$ may be brought back high only when LDCKA is low during the first two LDCKA cycles. $\overline{\text{PENA}}$ may be brought high at any time after the second LDCKA pulse returns low. A maximum value of 255 may be programmed for either X or Y. To use the default values of X = Y = 128 for AF/AEA, $\overline{\text{PENA}}$ must be tied high. No data is stored in the FIFO when its AF/AE offsets are programmed.

The AF/AEB flag is programmed in the same manner. $\overline{\text{PENB}}$ enables LDCKB to program the AF/AEB offset values taken from B0–B7.

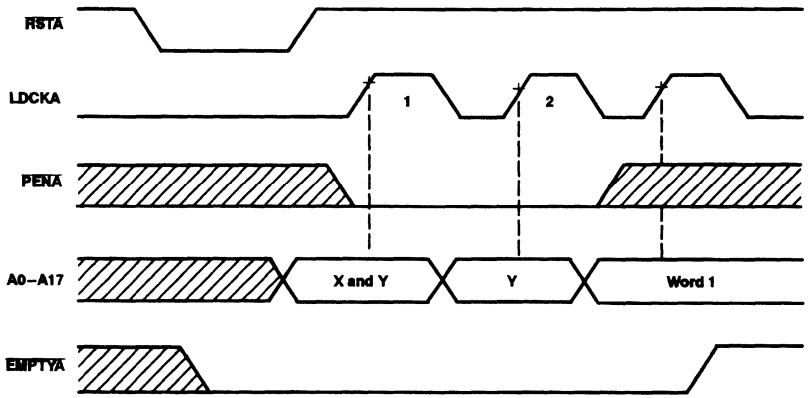



**Figure 1. Timing Diagram to Program X and Y Separately for AF/AEA**

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −0.5 V to $V_{CC}$ + 0.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$ ..... −0.5 V to 5.5 V
Current into any output in the low state, $I_O$ ..... 48 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... −18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | −12 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −3 mA | | 2.5 | | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = −3 mA | | 3 | | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −12 mA | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | | | 0.55 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | | ±5 | µA |
| $I_{OZH}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | µA |
| $I_{OZL}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | −50 | µA |
| $I_O$¶ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | | −40 | −100 | −180 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND, Outputs high | | | 15 | mA |
| | | | | $V_I$ = $V_{CC}$ or GND, Outputs low | | | 95 | |
| | | | | $V_I$ = $V_{CC}$ or GND, Outputs disabled | | | 15 | |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | | 6 | | pF |
| $C_o$ | Flags | $V_O$ = 2.5 V or 0.5 V | | | | 4 | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## timing characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | | | 'ABT7820-15 | | 'ABT7820-20 | | 'ABT7820-25 | | 'ABT7820-30 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 67 | | 50 | | 40 | | 33 | | MHz |
| $t_w$ | Pulse duration | LDCKA, LDCKB high | 4 | | 6 | | 9 | | 11 | | ns |
| | | LDCKA, LDCKB low | 4 | | 6 | | 9 | | 11 | | |
| | | UNCKA, UNCKB high | 4 | | 6 | | 9 | | 11 | | |
| | | UNCKA, UNCKB low | 4 | | 6 | | 9 | | 11 | | |
| | | $\overline{RSTA}$, $\overline{RSTB}$ low | 6 | | 8 | | 10 | | 12 | | |
| $t_{su}$ | Setup time | A0–A17 before LDCKA↑ and B0–B17 before LDCKB↑ | 3 | | 4 | | 4 | | 4 | | ns |
| | | $\overline{PENA}$ before LDCKA↑ and $\overline{PENB}$ before LDCKB↑ | 5 | | 5 | | 5 | | 5 | | |
| | | LDCKA inactive before $\overline{RSTA}$ high and LDCKB inactive before $\overline{RSTB}$ high | 3 | | 3 | | 4 | | 4 | | |
| $t_h$ | Hold time | A0–A17 after LDCKA↑ and B0–B17 after LDCKB↑ | 0 | | 0 | | 0 | | 0 | | ns |
| | | $\overline{PENA}$ after LDCKA low and $\overline{PENB}$ after LDCKB low | 2 | | 2 | | 2 | | 2 | | |
| | | LDCKA inactive after $\overline{RSTA}$ high and LDCKB inactive after $\overline{RSTB}$ high | 3 | | 3 | | 4 | | 4 | | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 4)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7820-15 | | | 'ACT7820-20 | | 'ACT7820-25 | | 'ACT7820-30 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK, UNCK | | | | 67 | | 50 | | 40 | | 33.3 | MHz |
| $t_{pd}$ | LDCKA↑, LDCKB↑ | B/A | 4 | | 14 | 4 | 15 | 4 | 18 | 4 | 20 | ns |
| | UNCKA↑, UNCKB↑ | | 4 | 9 | 12 | 4 | 13.5 | 4 | 15 | 4 | 17 | |
| $t_{pd}$¶ | UNCKA↑, UNCKB↑ | B/A | | 8 | | | | | | | | ns |
| $t_{PLH}$ | LDCKA↑, LDCKB↑ | EMPTYA, EMPTYB | 4 | | 14 | 4 | 15 | 4 | 17 | 4 | 19 | ns |
| $t_{PHL}$ | UNCKA↑, UNCKB↑ | | 4 | | 13 | 4 | 14 | 4 | 16 | 4 | 18 | |
| $t_{PHL}$ | $\overline{RSTA}$ low, $\overline{RSTB}$ low | EMPTYA, EMPTYB | 6 | | 16 | 6 | 16 | 6 | 18 | 6 | 20 | ns |
| $t_{PHL}$ | LDCKA↑, LDCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 6 | | 13 | 6 | 14 | 6 | 16 | 6 | 18 | ns |
| $t_{PLH}$ | UNCKA↑, UNCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 6 | | 15 | 6 | 15 | 6 | 17 | 6 | 19 | ns |
| | $\overline{RSTA}$ low, $\overline{RSTB}$ low | | 8 | | 20 | 8 | 20 | 8 | 22 | 8 | 22 | |
| $t_{pd}$ | LDCKA↑, LDCKB↑ | AF/AEA, AF/AEB | 8 | | 16 | 8 | 17 | 8 | 18 | 8 | 20 | ns |
| | UNCKA↑, UNCKB↑ | | 8 | | 16 | 8 | 17 | 8 | 18 | 8 | 20 | |
| $t_{PLH}$ | $\overline{RSTA}$ low, $\overline{RSTB}$ low | AF/AEA, AF/AEB | 2 | | 12 | 2 | 14 | 2 | 16 | 2 | 18 | ns |
| $t_{PLH}$ | LDCKA↑, LDCKB↑ | HFA, HFB | 8 | | 15 | 8 | 15 | 8 | 17 | 8 | 19 | ns |
| $t_{PHL}$ | UNCKA, UNCKB | HFA, HFB | 8 | | 15 | 8 | 15 | 8 | 17 | 8 | 19 | ns |
| | $\overline{RSTA}$ low, $\overline{RSTB}$ low | | 2 | | 12 | 2 | 14 | 2 | 16 | 2 | 18 | |
| $t_{pd}$ | SAB/SBA§ | B/A | 2 | | 10 | 2 | 11 | 2 | 12 | 2 | 14 | ns |
| | A/B | | 2 | | 9 | 2 | 10 | 2 | 11 | 2 | 13 | |
| $t_{en}$ | GBA/GAB | A/B | 2 | | 6.5 | 2 | 8 | 2 | 10 | 2 | 12 | ns |
| $t_{dis}$ | GBA/GAB | A/B | 2 | | 11 | 2 | 12 | 2 | 13 | 2 | 14 | ns |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at 5 V, $T_A$ = 25°C.
¶ This parameter is measured with a 30-pF load (see Figure 2).
§ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

## TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

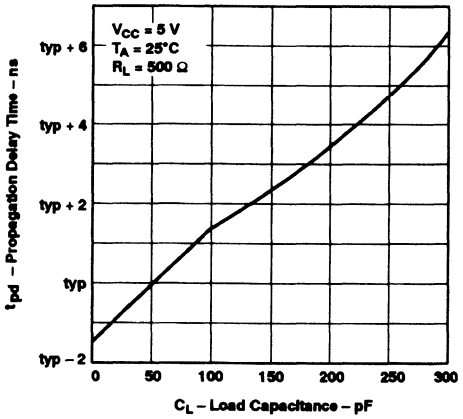



Figure 2

SUPPLY CURRENT
vs
CLOCK FREQUENCY

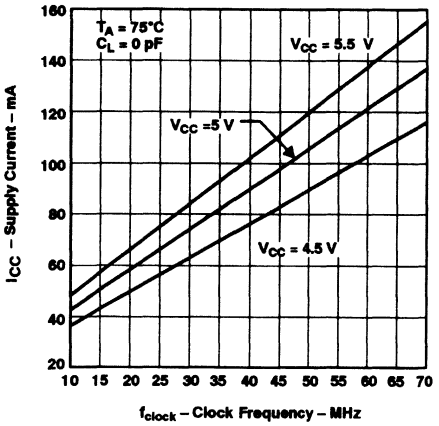



Figure 3

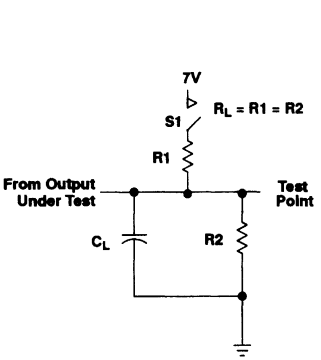
### calculating power dissipation

With $I_{CCF}$ taken from Figure 3, the maximum power dissipation based on all outputs changing states on each read may be calculated using:

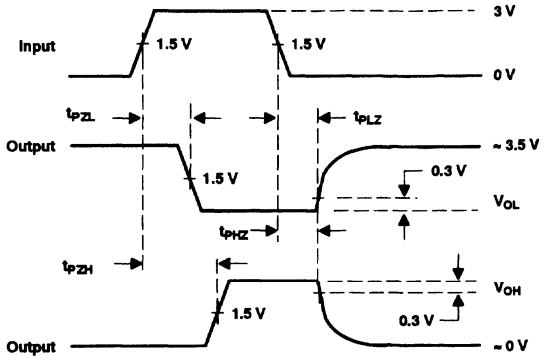
$$P_t = V_{CC} \times [I_{CCF}] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CCF}$ = maximum $I_{CC}$ per clock frequency
$C_L$ = output capacitive load
$f_o$ = data output frequency

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

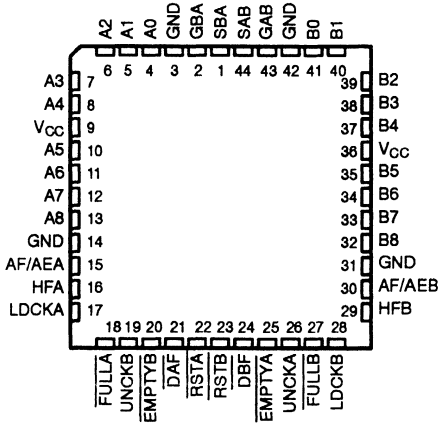
† Includes probe and test fixture capacitance.

**Figure 4. Load Circuit and Voltage Waveforms**

SCAS148A–D3568, DECEMBER 1990–REVISED APRIL 1991

- **Independent Asynchronous Inputs and Outputs**
- **Low-Power Advanced CMOS Technology**
- **Bidirectional**
- **1024 Words by 9 Bits Each**
- **Programmable Almost Full/Almost Empty Flag**
- **Empty, Full, and Half-Full Flags**
- **Access Times of 25 ns With a 50-pF Load**
- **Data Rates From 0 to 50 MHz**
- **Fall-Through Times of 22 ns Max**
- **High Output Drive for Direct Bus Interface**

**FN PACKAGE**
**(TOP VIEW)**




## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT2235 is arranged as two 1024 by 9-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 50 MHz with access times of 25 ns in a bit-parallel format.

The SN74ACT2235 consists of bus transceiver circuits, two 1024 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable GAB and GBA inputs are provided to control the transceiver functions. The SAB and SBA control inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Eight fundamental bus-management functions can be performed as shown on the operating modes page.

## functional description

**bus lines (A0–A8, B0–B8)**

Data inputs and outputs for 9-bit wide data.

**resets ($\overline{RSTA}$, $\overline{RSTB}$)**

A reset is accomplished in each direction by taking reset ($\overline{RSTA}$) and ($\overline{RSTB}$) low. This sets the empty flags ($\overline{EMPTYA}$ and $\overline{EMPTYB}$) and the half-full flags (HFA and HFB) low. The full flags ($\overline{FULLA}$ and $\overline{FULLB}$) and the almost full/almost empty flags (AF/AEA and AF/AEB) are set high. Both FIFOs must be reset upon power up.

**load clocks (LDCKA, LDCKB)**

Data on the A bus (A0–A8) is written into FIFO A on a low-to-high transition of load clock A (LDCKA). Data on the B bus (B0–B8) is written into FIFO B on a low-to-high transition of load clock B (LDCKB). When the FIFOs are full, load clock signals have no effect on the data residing in memory.

**unload clocks (UNCKA, UNCKB)**

Data in FIFO A is read to the B bus (B0–B8) on a low-to-high transition of unload clock A (UNCKA). Data in FIFO B is read to the A bus (A0–A8) on a low-to-high transition of unload clock B(UNCKB). When the FIFOs are empty, unload clock signals have no effect on data residing in memory.

**output enables (GAB, GBA)**

The output enables (GAB, GBA) control the transceiver functions. When GBA is low, the A bus (A0–A8) is in the high-impedance state. When GAB is low, the B bus (B0–B8) is in the high-impedance state.

**select control inputs (SAB, SBA)**

The s-control inputs (SAB, SBA) select whether real-time or stored data is transferred. A low level selects real-time data, and a high level selects stored data. Eight fundamental bus-management functions can be performed as shown on the operating modes page.

**define flag inputs ($\overline{DAF}$, $\overline{DBF}$)**

The high-to-low transition of define A flag ($\overline{DAF}$) stores the binary value on the A bus (A0–A8) as the almost full/almost empty offset value for FIFO A (X). The high-to-low transition of define B flag ($\overline{DBF}$) stores the binary value of the B bus (B0–B8) as the almost full/almost empty offset value for FIFO B (Y).

**empty flags ($\overline{EMPTYA}$, $\overline{EMPTYB}$)**

The empty flags ($\overline{EMPTYA}$, $\overline{EMPTYB}$) will be low when their corresponding memories are empty, and high when they are not empty.

**full flags ($\overline{FULLA}$, $\overline{FULLB}$)**

The full flags ($\overline{FULLA}$, $\overline{FULLB}$) will be low when their corresponding memories are full, and high when they are not full.

**half-full flags (HFA, HFB)**

The half-full flags (HFA and HFB) are high when their corresponding memories contain 512 or more words, and low when they contain 511 or less words.

**almost full/almost empty flags (AF/AEA, AF/AEB)**

The almost full/almost empty A flag (AF/AEA) is defined by the almost full/almost empty offset value for FIFO A (X). The AF/AEA flag is high when FIFO A contains X or less words or 1024 minus X words. The AF/AEA flag is low when FIFO A contains between X plus 1 or 1023 minus X words. The operation of the almost full/almost empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.

## functional description (continued)

### programming procedure for AF/AEA

The almost full/almost empty flags (AF/AEA, AF/AEB) are programmed during each reset cycle. The almost full/almost empty offset value FIFO A (X) and for FIFO B (Y) are either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

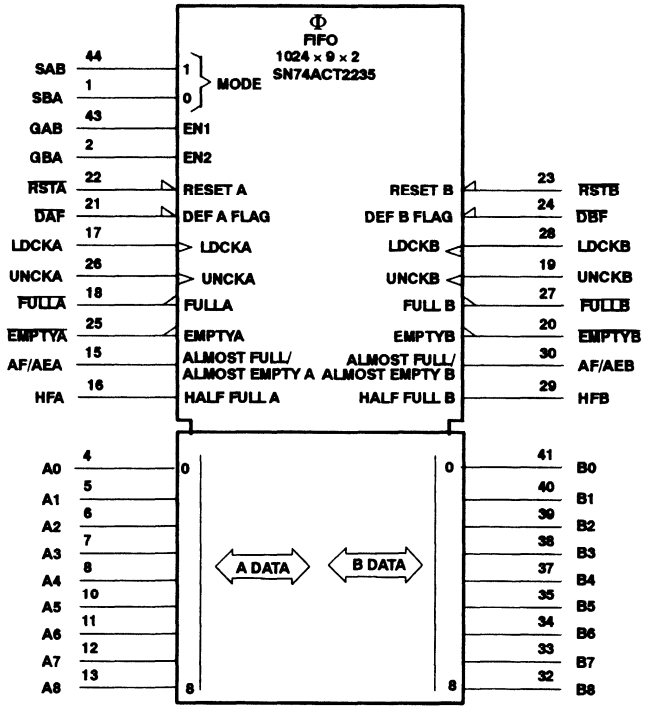
***user-defined X***

Step 1. Take $\overline{DAF}$ from high to low. This stores A0 thru A8 as X.
Step 2. If $\overline{RSTA}$ is not already low, take $\overline{RSTA}$ low.
Step 3. With $\overline{DAF}$ held low, take $\overline{RSTA}$ high. This defines the AF/AEA flag using X.
Step 4. To retain the current offset for the next reset, keep $\overline{DAF}$ low.

***default X***

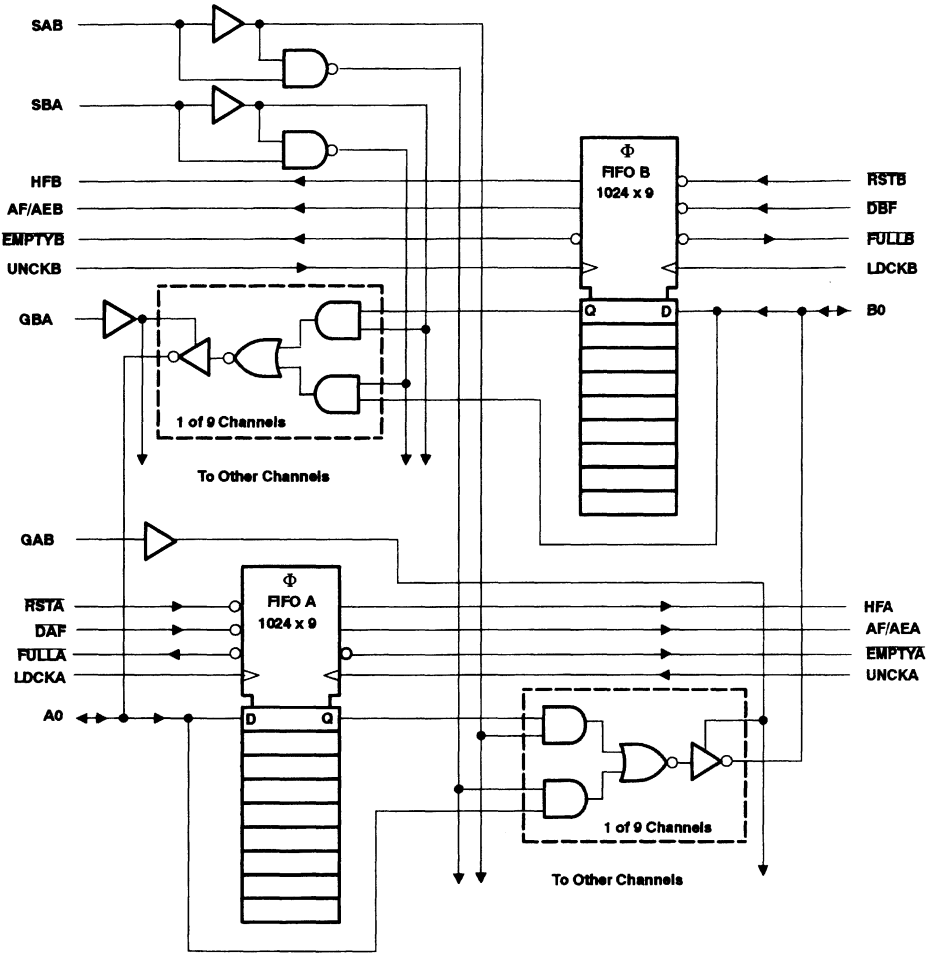
To redefine the AF/AE flag using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.

## logic symbol†

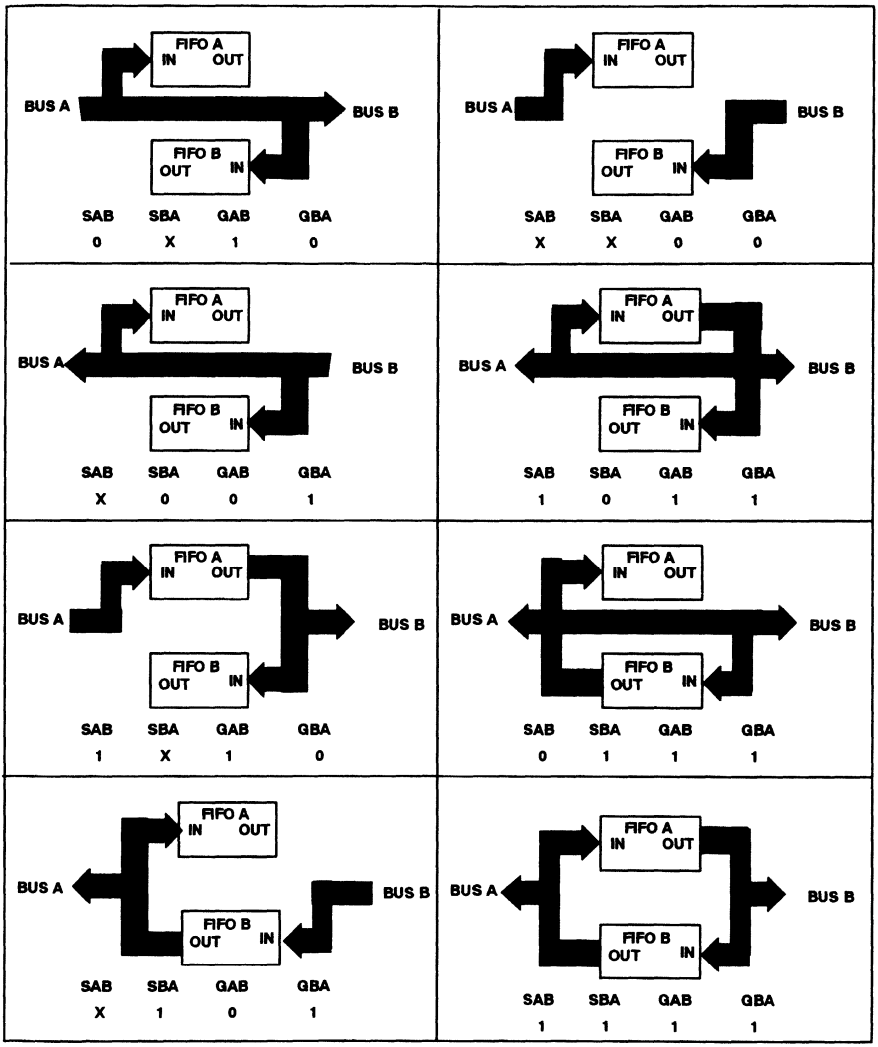



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

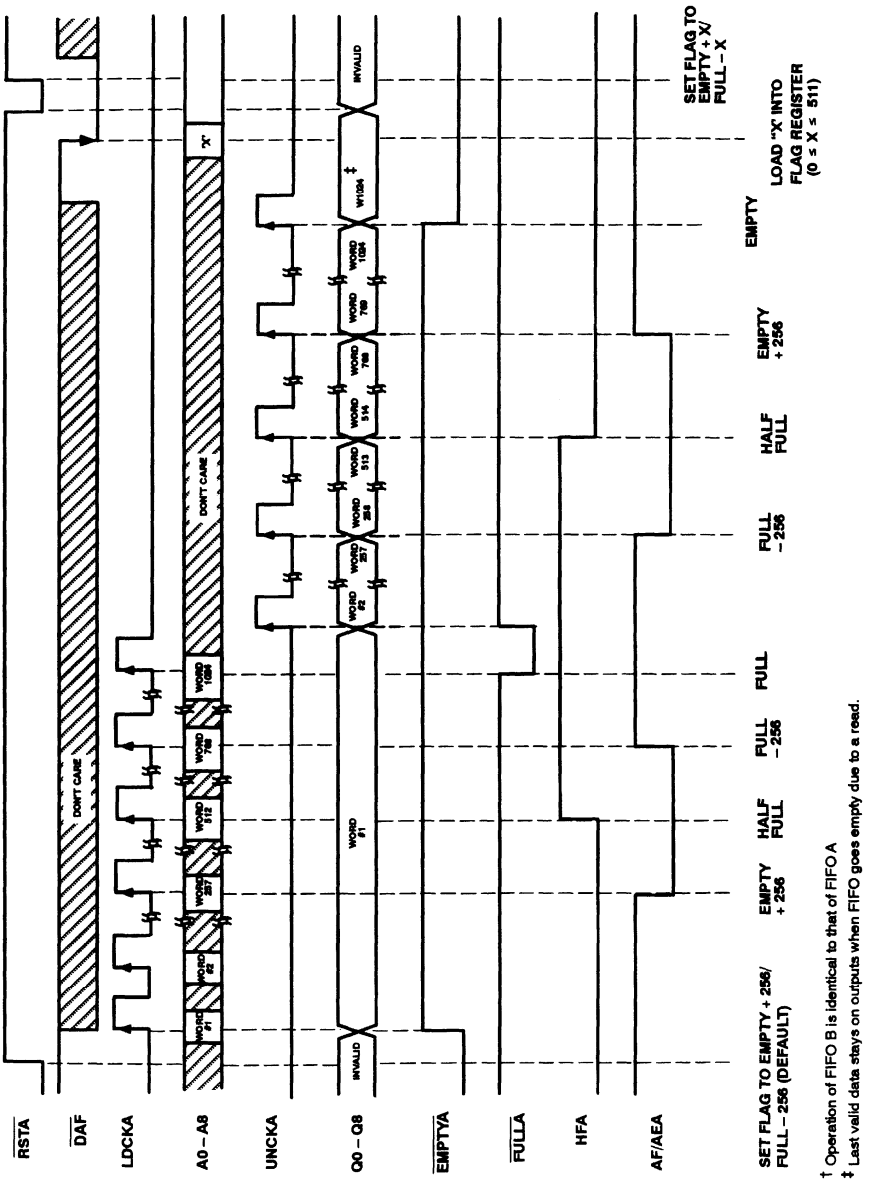
## logic diagram (positive logic)



## operating modes



## timing diagram, FIFO A†




† Operation of FIFO B is identical to that of FIFO A

‡ Last valid data stays on outputs when FIFO goes empty due to a read.

SELECT-MODE CONTROL TABLE

| CONTROL | | OPERATION | |
|---|---|---|---|
| SAB | SBA | A BUS | B BUS |
| L | L | Real-time B to A bus | Real-time A to B bus |
| L | H | FIFO B to A bus | Real-time A to B bus |
| H | L | Real-time B to A bus | FIFO A to B bus |
| H | H | FIFO B to A bus | FIFO A to B bus |

OUTPUT-ENABLE CONTROL TABLE

| CONTROL | | OPERATION | |
|---|---|---|---|
| GAB | GBA | A BUS | B BUS |
| H | H | A bus enabled | B bus enabled |
| L | H | A bus enabled | Isolation/input to B bus |
| H | L | Isolation/input to A bus | B bus enabled |
| L | L | Isolation/input to A bus | Isolation/input to B bus |

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage: Control inputs ..... 7 V
I/O ports ..... 5.5 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Maximum junction temperature ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | 'ACT2235-20 | | 'ACT2235-30 | | 'ACT2235-40 | | 'ACT2235-60 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | A or B ports | | −8 | | −8 | | −8 | | −8 | mA |
| | | Status flags | | −8 | | −8 | | −8 | | −8 | |
| $I_{OL}$ | Low-level output current | A or B ports | | 16 | | 16 | | 16 | | 16 | mA |
| | | Status flags | | 8 | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | LDCKA or LDCKB | | 50 | | 33 | | 25 | | 16.7 | MHz |
| | | UNCKA or UNCKB | | 50 | | 33 | | 25 | | 16.7 | |
| $t_w$ | Pulse duration | $\overline{RSTA}$ or $\overline{RSTB}$ low | 20 | | 20 | | 25 | | 25 | | ns |
| | | LDCKA or LDCKB low | 8 | | 10 | | 14 | | 20 | | |
| | | LDCKA or LDCKB high | 8 | | 10 | | 14 | | 20 | | |
| | | UNCKA or UNCKB low | 8 | | 10 | | 14 | | 20 | | |
| | | UNCKA or UNCKB high | 8 | | 10 | | 14 | | 20 | | |
| | | $\overline{DAF}$ or $\overline{DBF}$ high | 10 | | 10 | | 10 | | 10 | | |
| $t_{su}$ | Setup time | Data before LDCKA or LDCKB↑ | 4 | | 4 | | 5 | | 5 | | ns |
| | | Define AF/AE: D0–D8 before $\overline{DAF}$ or $\overline{DBF}$↓ | 5 | | 5 | | 5 | | 5 | | |
| | | Define AF/AE: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 7 | | 7 | | 7 | | 7 | | |
| | | Define AF/AE (default): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 5 | | 5 | | 5 | | 5 | | |
| | | $\overline{RSTA}$ or $\overline{RSTB}$ inactive (high) before LDCKA or LDCKB↑ | 5 | | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time | Data after LDCKA or LDCKB↑ | 1 | | 1 | | 2 | | 2 | | ns |
| | | Define AF/AE: D0–D8 after $\overline{DAF}$ or $\overline{DBF}$↓ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE (default): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | 0 | | 0 | | 0 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | I/O ports | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$‡ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | 10 | 400 | μA |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ $I_{CC}$ tested with outputs open.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

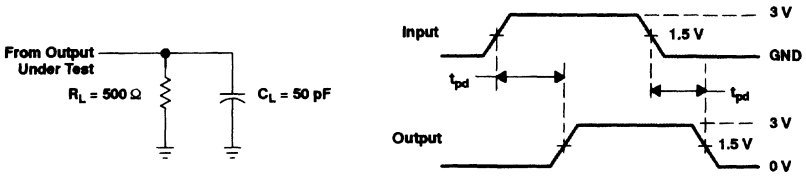
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT2235-20 | | | 'ACT2235-30 | | 'ACT2235-40 | | 'ACT2235-60 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK | | 50 | | | 33 | | 25 | | 16.7 | | MHz |
| | UNCK | | 50 | | | 33 | | 25 | | 16.7 | | |
| $t_{pd}$ | LDCK↑, LDCKB↑ | B or A | 8 | | 22 | 8 | 22 | 8 | 24 | 8 | 26 | ns |
| $t_{pd}$ | UNCKA↑, UNCKB↑ | B or A | 12 | 17 | 25 | 12 | 25 | 12 | 35 | 12 | 45 | ns |
| $t_{PLH}$ | LDCK↑, LDCKB↑ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 4 | | 15 | 4 | 15 | 4 | 17 | 4 | 19 | ns |
| $t_{PHL}$ | UNCKA↑, UNCKB↑ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 2 | | 17 | 2 | 17 | 2 | 19 | 2 | 21 | ns |
| $t_{PHL}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 2 | | 18 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| $t_{PHL}$ | LDCK↑, LDCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 4 | | 15 | 4 | 15 | 4 | 17 | 4 | 19 | ns |
| $t_{PLH}$ | UNCKA↑, UNCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 4 | | 15 | 4 | 15 | 4 | 17 | 4 | 19 | ns |
| $t_{PLH}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | $\overline{FULLA}$, $\overline{FULLB}$ | 2 | | 15 | 2 | 15 | 2 | 17 | 2 | 19 | ns |
| $t_{PLH}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | AF/AEA, AF/AEB | 2 | | 15 | 2 | 15 | 2 | 17 | 2 | 19 | ns |
| $t_{PLH}$ | LDCK↑, LDCKB↑ | HFA, HFB | 2 | | 15 | 2 | 15 | 2 | 17 | 2 | 19 | ns |
| $t_{PHL}$ | UNCKA↑, UNCKB↑ | HFA, HFB | 4 | | 18 | 4 | 18 | 4 | 20 | 4 | 22 | ns |
| $t_{PHL}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | HFA, HFB | 1 | | 15 | 1 | 15 | 1 | 17 | 1 | 19 | ns |
| $t_{pd}$ | SAB or SBA¶ | B or A | 1 | | 11 | 1 | 11 | 1 | 12 | 1 | 14 | ns |
| $t_{pd}$ | A or B | B or A | 1 | | 11 | 1 | 11 | 1 | 12 | 1 | 14 | ns |
| $t_{pd}$ | LDCK↑, LDCKB↑ | AF/AEA, AF/AEB | 2 | | 18 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| $t_{pd}$ | UNCKA↑, UNCKB↑ | AF/AEA, AF/AEB | 2 | | 18 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| $t_{en}$ | GBA or GAB | A or B | 2 | | 11 | 2 | 11 | 2 | 13 | 2 | 15 | ns |
| $t_{dis}$ | GBA or GAB | A or B | 1 | | 9 | 1 | 9 | 1 | 11 | 1 | 13 | ns |

¶ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per 1 Kbits | Outputs enabled | $C_L$ = 50 pF, f = 5 MHz | 71 | pF |
| | | Outputs disabled | | 57 | |

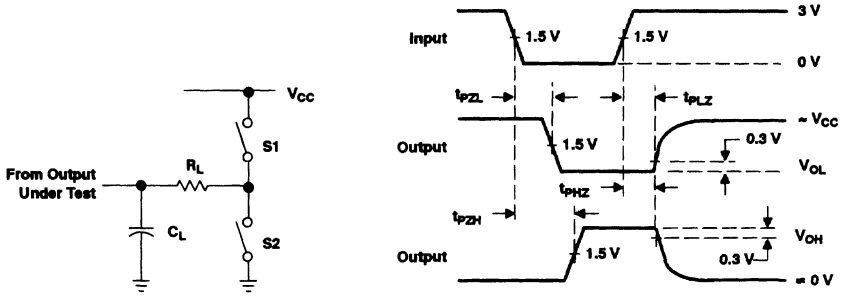
## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT

TOTEM-POLE OUTPUTS

**Figure 1. Standard CMOS Outputs (All Flags)**




LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

| PARAMETER | | $R_L$ | $C_L$† | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | – | 50 pF | Open | Open |

† Includes probe and test fixture capacitance.

**Figure 2. 3-State Outputs (A0–A8, B0–B8)**

## TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

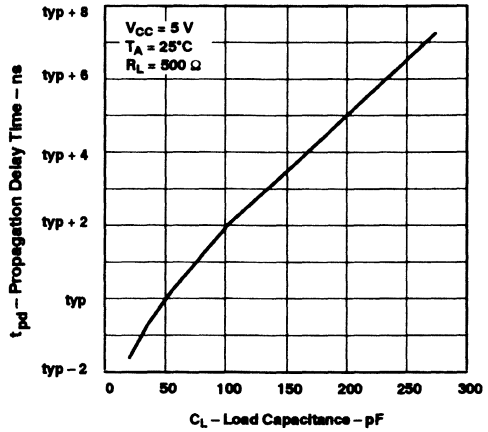



Figure 3

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

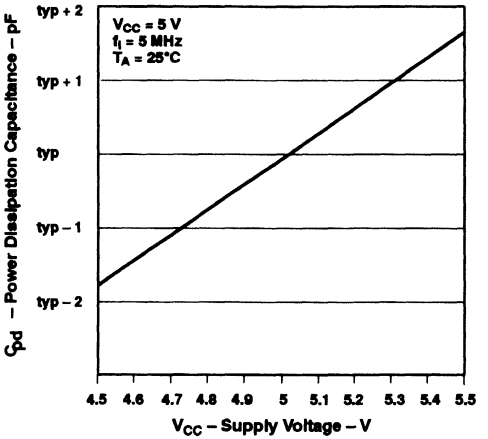



Figure 4

### calculating power dissipation

With $I_{CCF}$ taken from Figure 4, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

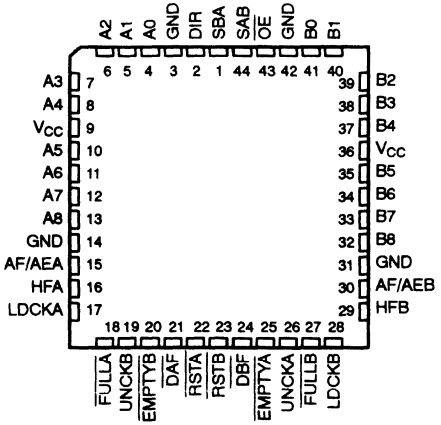
$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\ (C_{pd} \times V_{CC}^2 \times fi) + \Sigma\ (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta\ I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

SCAS149–D3489, APRIL 1990–REVISED DECEMBER 1990

- Independent Asynchronous Inputs and Outputs
- Low-Power Advanced CMOS Technology
- Bidirectional
- 1024 Words by 9 Bits Each
- Programmable Almost Full/Almost Empty Flag
- Empty, Full, and Half-Full Flags
- Access Times of 25 ns With a 50-pF Load
- Data Rates From 0 to 50 MHz
- Fall-Through Times of 23 ns Max
- High Output Drive for Direct Bus Interface
- 3-State Outputs

FN PACKAGE
(TOP VIEW)




## description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT2236 is arranged as two 1024 by 9-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 50 MHz with access times of 25 ns in a bit-parallel format.

The SN74ACT2236 consists of bus transceiver circuits, two 1024 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable $\overline{OE}$ and DIR inputs are provided to control the transceiver functions. The SAB and SBA control inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Five fundamental bus-management functions can be performed as shown on the operating modes page.

## functional description

**bus lines (A0–A8, B0–B8)**

Data inputs and outputs for 9-bit wide data.

**resets ($\overline{RSTA}$, $\overline{RSTB}$)**

A reset is accomplished in each direction by taking reset ($\overline{RSTA}$) and ($\overline{RSTB}$) low. This sets the empty flags ($\overline{EMPTYA}$ and $\overline{EMPTYB}$) and the half-full flags (HFA and HFB) low. The full flags ($\overline{FULLA}$ and $\overline{FULLB}$) and the almost full/almost empty flags (AF/AEA and AF/AEB) are set high. Both FIFOs must be reset upon power up.

**load clocks (LDCKA, LDCKB)**

Data on the A bus (A0–A8) is written into FIFO A on a low-to-high transition of load clock A (LDCKA). Data on the B bus (B0–B8) is written into FIFO B on a low-to-high transition of load clock B (LDCKB). When the FIFOs are full, load clock signals have no effect on the data residing in memory.

**unload clocks (UNCKA, UNCKB)**

Data in FIFO A is read to the B bus (B0–B8) on a low-to-high transition of unload clock A (UNCKA). Data in FIFO B is read to the A bus (A0–A8) on a low-to-high transition of unload clock B (UNCKB). When the FIFOs are empty, unload clock signals have no effect on data residing in memory.

**enable inputs ($\overline{OE}$, DIR)**

The enable inputs control the transceiver functions. When $\overline{OE}$ is high, both buses (A0–A8, B0–B8) are in the high-impedance state and may be used as inputs. With $\overline{OE}$ low and DIR high, the A bus is in the high-impedance state and B bus is active. When both $\overline{OE}$ and DIR are low, the A bus is active and the B bus is in the high-impedance state.

**select control inputs (SAB, SBA)**

The select control inputs (SAB, SBA) select whether real-time or stored data is transferred. A low level selects real-time data, and a high level selects stored data. Five fundamental bus-management functions can be performed as shown on the operating modes page.

**define flag inputs ($\overline{DAF}$, $\overline{DBF}$)**

The high-to-low transition of define A flag ($\overline{DAF}$) stores the binary value on the A bus (A0–A8) as the almost full/almost empty offset value for FIFO A (X). The high-to-low transition of define B flag ($\overline{DBF}$) stores the binary value of the B bus (B0–B8) as the almost full/almost empty offset value for FIFO B (Y).

**empty flags ($\overline{EMPTYA}$, $\overline{EMPTYB}$)**

The empty flags ($\overline{EMPTYA}$, $\overline{EMPTYB}$) will be low when their corresponding memories are empty, and high when they are not empty.

**full flags ($\overline{FULLA}$, $\overline{FULLB}$)**

The full flags ($\overline{FULLA}$, $\overline{FULLB}$) will be low when their corresponding memories are full, and high when they are not full.

**half-full flags (HFA, HFB)**

The half-full flags (HFA and HFB) are high when their corresponding memories contain 512 or more words, and low when they contain 511 or less words.

**almost full/almost empty flags (AF/AEA, AF/AEB)**

The almost full/almost empty A flag (AF/AEA) is defined by the almost full/almost empty offset value for FIFO A (X). The AF/AEA flag is high when FIFO A contains X or less words or 1024 minus X words. The AF/AEA flag is low when FIFO A contains between X plus 1 or 1023 minus X words. The operation of the almost full/almost empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.

## functional description (continued)

### programming procedure for AF/AEA

The almost full/almost empty flags (AF/AEA, AF/AEB) are programmed during each reset cycle. The almost full/almost empty offset value FIFO A (X) and for FIFO B (Y) are either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

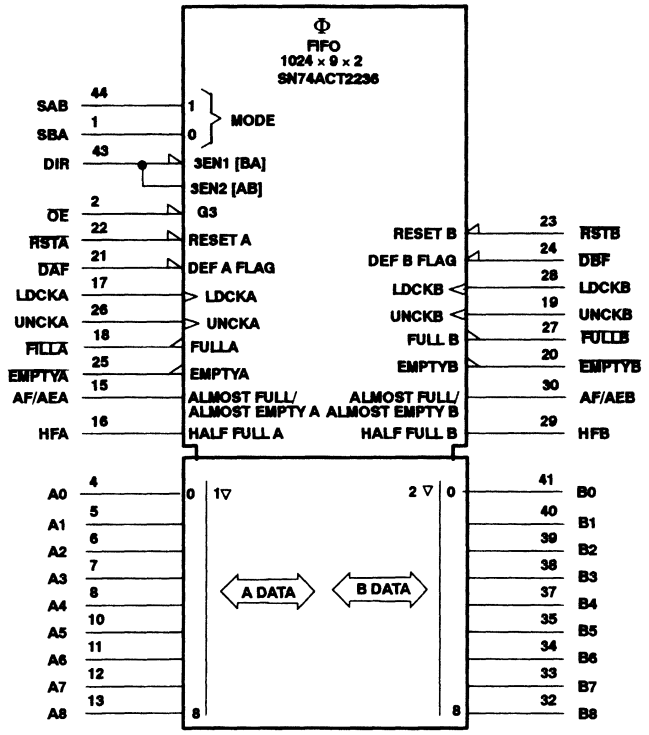
***user-defined X***

Step 1. Take $\overline{DAF}$ from high to low. This stores A0 thru A8 as X.
Step 2. If $\overline{RSTA}$ is not already low, take $\overline{RSTA}$ high.
Step 3. With $\overline{DAF}$ held low, take $\overline{RSTA}$ high. This defines the AF/AEA flag using X.
Step 4. To retain the current offset for the next reset, keep $\overline{DAF}$ low.

***default X***

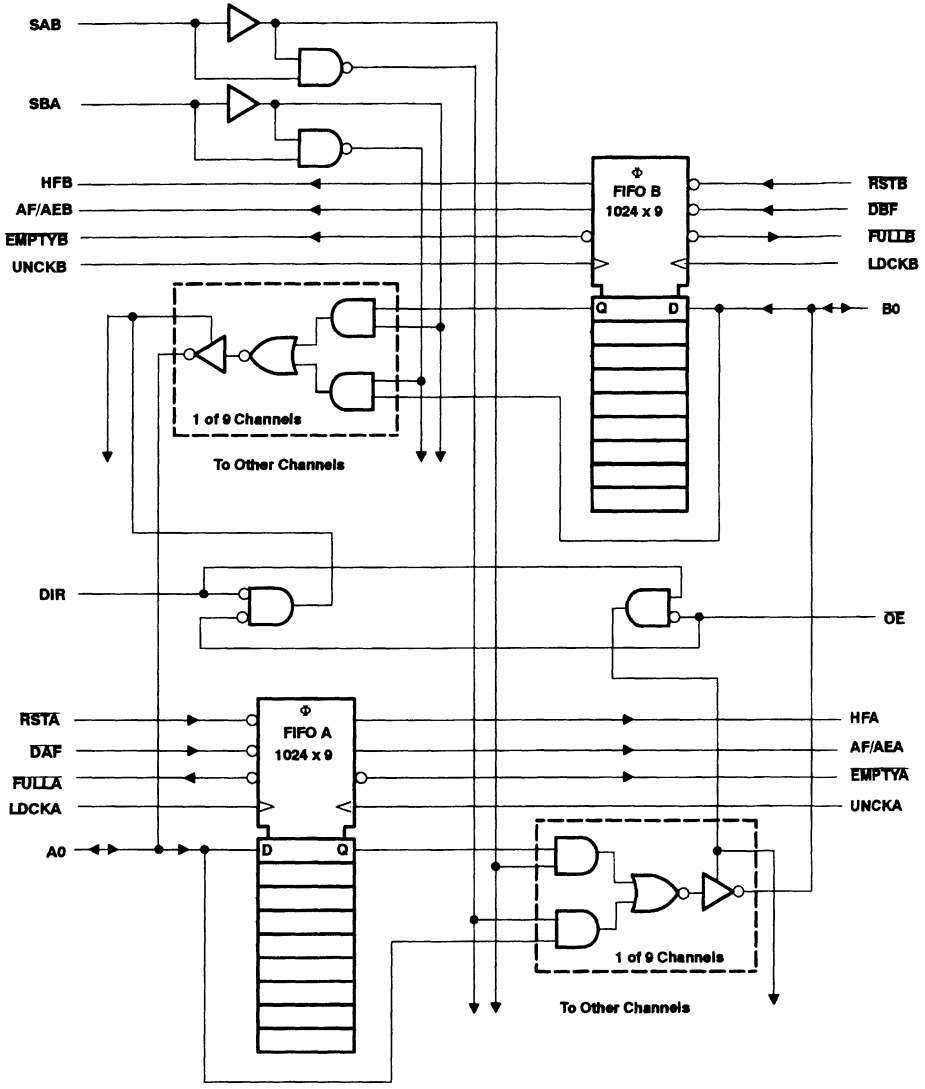
To redefine the AF/AE flag using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984.

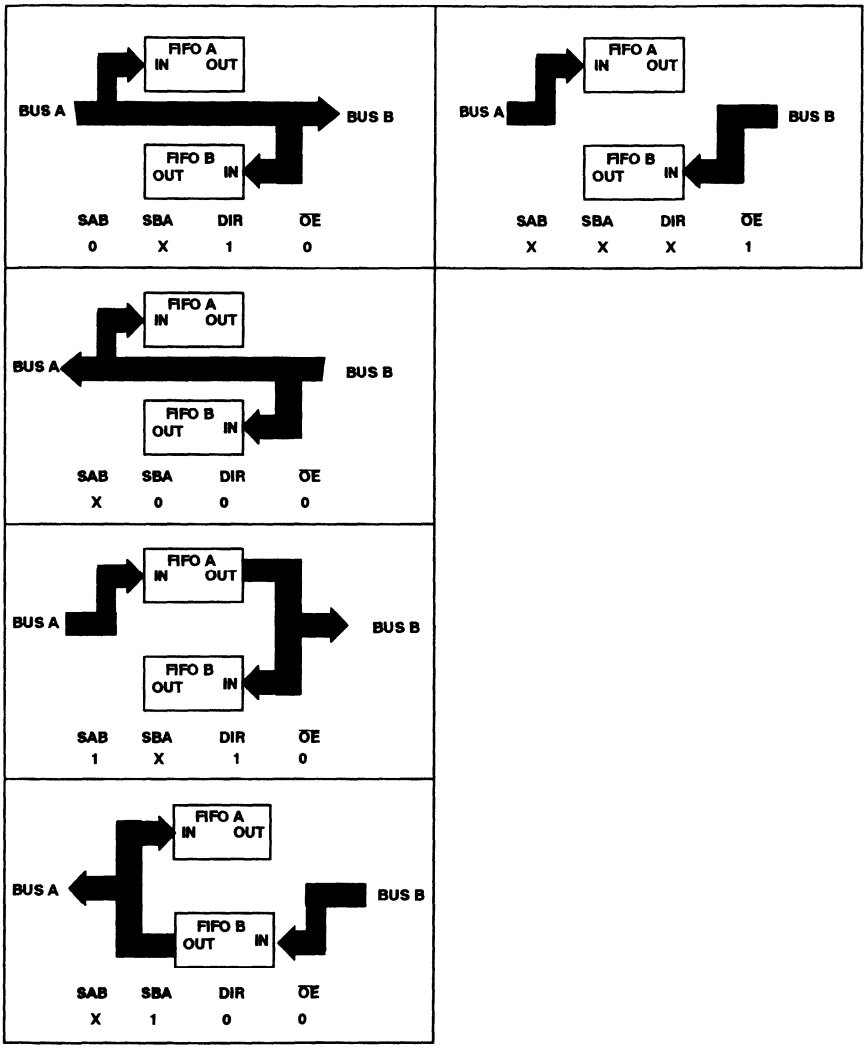
## logic diagram (positive logic)





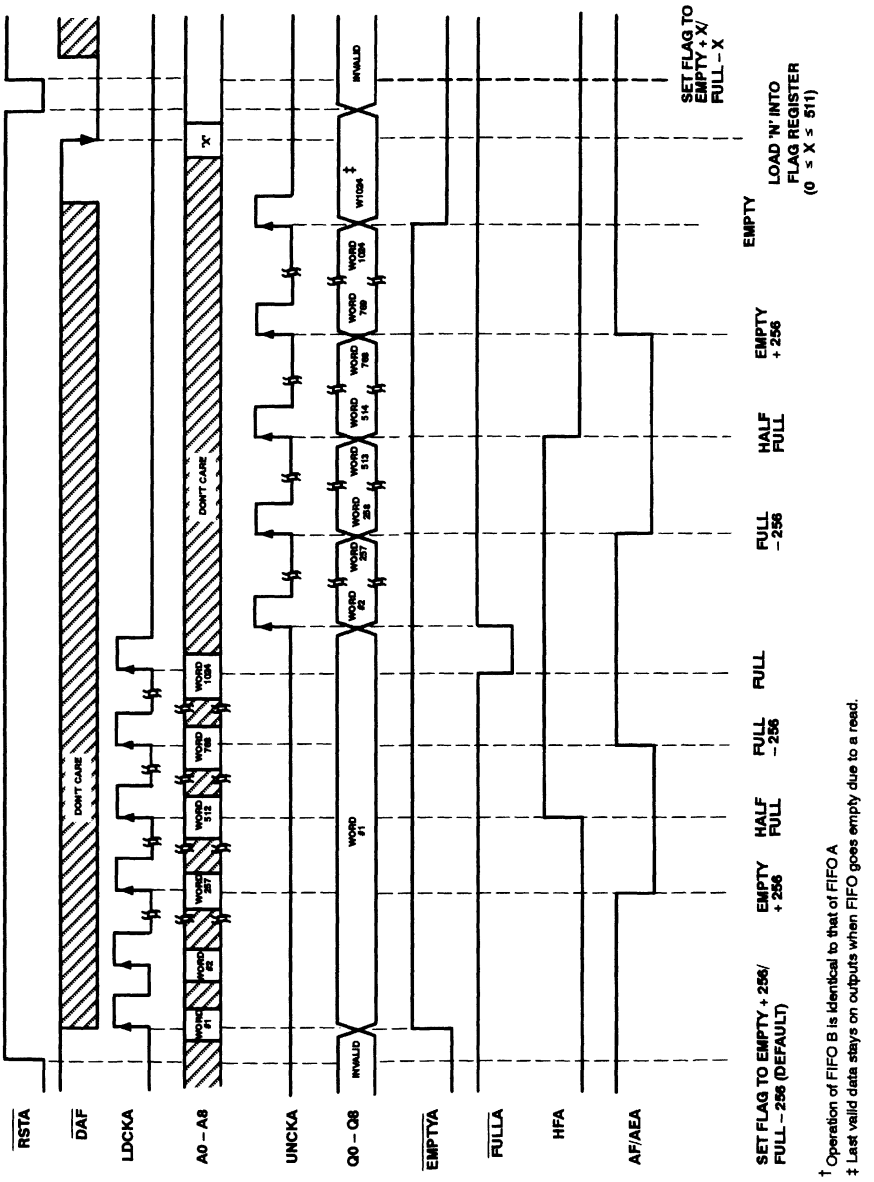

TEXAS INSTRUMENTS

## operating modes



SCAS149–D3489, APRIL 1990–REVISED DECEMBER 1990

## timing diagram, FIFO A†




† Operation of FIFO B is identical to that of FIFO A

‡ Last valid data stays on outputs when FIFO goes empty due to a read.

**SELECT-MODE CONTROL TABLE**

| CONTROL | | OPERATION | |
|---|---|---|---|
| SAB | SBA | A BUS | B BUS |
| L | L | Real-time B to A bus | Real-time A to B bus |
| L | H | FIFO B to A bus | Real-time A to B bus |
| H | L | Real-time B to A bus | FIFO A to B bus |
| H | H | FIFO B to A bus | FIFO A to B bus |

**OUTPUT-ENABLE CONTROL TABLE**

| CONTROL | | OPERATION | |
|---|---|---|---|
| DIR | $\overline{OE}$ | A BUS | B BUS |
| X | H | Input | Input |
| L | L | Output | Input |
| H | L | Input | Output |

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage: Control inputs ..... 7 V
I/O ports ..... 5.5 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Maximum junction temperature ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | 'ACT2236-20 | | 'ACT2236-30 | | 'ACT2236-40 | | 'ACT2236-60 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | A or B ports | | −8 | | −8 | | −8 | | −8 | mA |
| | | Status flags | | −8 | | −8 | | −8 | | −8 | |
| $I_{OL}$ | Low-level output current | A or B ports | | 16 | | 16 | | 16 | | 16 | mA |
| | | Status flags | | 8 | | 8 | | 8 | | 8 | |
| $f_{clock}$ | Clock frequency | LDCKA or LDCKB | | 50 | | 33 | | 25 | | 16.7 | MHz |
| | | UNCKA or UNCKB | | 50 | | 33 | | 25 | | 16.7 | |
| $t_w$ | Pulse duration | $\overline{RSTA}$ or $\overline{RSTB}$ low | 20 | | 20 | | 25 | | 25 | | ns |
| | | LDCKA or LDCKB low | 8 | | 10 | | 14 | | 20 | | |
| | | LDCKA or LDCKB high | 8 | | 10 | | 14 | | 20 | | |
| | | UNCKA or UNCKB low | 8 | | 10 | | 14 | | 20 | | |
| | | UNCKA or UNCKB high | 8 | | 10 | | 14 | | 20 | | |
| | | $\overline{DAF}$ or $\overline{DBF}$ high | 10 | | 10 | | 10 | | 10 | | |
| $t_{su}$ | Setup time | Data before LDCKA or LDCKB↑ | 4 | | 4 | | 5 | | 5 | | ns |
| | | Define AF/AE: D0–D8 before $\overline{DAF}$ or $\overline{DBF}$↓ | 5 | | 5 | | 5 | | 5 | | |
| | | Define AF/AE: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 7 | | 7 | | 7 | | 7 | | |
| | | Define AF/AE (default): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 5 | | 5 | | 5 | | 5 | | |
| | | $\overline{RSTA}$ or $\overline{RSTB}$ inactive (high) before LDCKA or LDCKB↑ | 5 | | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time | Data after LDCKA or LDCKB↑ | 1 | | 1 | | 2 | | 2 | | ns |
| | | Define AF/AE: D0–D8 after $\overline{DAF}$ or $\overline{DBF}$↓ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | 0 | | 0 | | 0 | | |
| | | Define AF/AE (default): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | 0 | | 0 | | 0 | | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | 0 | 70 | 0 | 70 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | I/O ports | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$‡ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | 10 | 400 | μA |
| $\Delta I_{CC}$§ | DIR, $\overline{OE}$ | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 2 | mA |
| | Other inputs | | | | | 1 | |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ $I_{CC}$ tested with outputs open.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

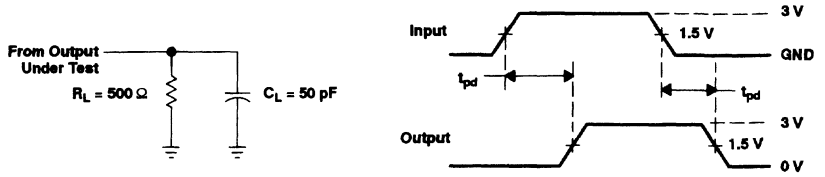
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT2236-20 | | | 'ACT2236-30 | | 'ACT2236-40 | | 'ACT2236-60 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | LDCK | | 50 | | | 33 | | 25 | | 16.7 | | MHz |
| | UNCK | | 50 | | | 33 | | 25 | | 16.7 | | |
| $t_{pd}$ | LDCK↑, LDCKB↑ | B or A | 8 | | 23 | 8 | 23 | 8 | 25 | 8 | 27 | ns |
| $t_{pd}$ | UNCKA↑, UNCKB↑ | B or A | 10 | 17 | 25 | 10 | 25 | 10 | 35 | 10 | 45 | ns |
| $t_{PLH}$ | LDCK↑, LDCKB↑ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 4 | | 15 | 4 | 15 | 4 | 17 | 4 | 19 | ns |
| $t_{PHL}$ | UNCKA↑, UNCKB↑ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 2 | | 17 | 2 | 17 | 2 | 19 | 2 | 21 | ns |
| $t_{PHL}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 2 | | 18 | 2 | 18 | 2 | 20 | 2 | 22 | ns |
| $t_{PHL}$ | LDCK↑, LDCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 4 | | 15 | 4 | 15 | 4 | 17 | 4 | 19 | ns |
| $t_{PLH}$ | UNCKA↑, UNCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 4 | | 15 | 4 | 15 | 4 | 17 | 4 | 19 | ns |
| $t_{PLH}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | $\overline{FULLA}$, $\overline{FULLB}$ | 2 | | 15 | 2 | 15 | 2 | 17 | 2 | 19 | ns |
| $t_{PLH}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | AF/AEA, AF/AEB | 2 | | 15 | 2 | 15 | 2 | 17 | 2 | 19 | ns |
| $t_{PLH}$ | LDCK↑, LDCKB↑ | HFA, HFB | 2 | | 15 | 2 | 15 | 2 | 17 | 2 | 19 | ns |
| $t_{PHL}$ | UNCKA↑, UNCKB↑ | HFA, HFB | 4 | | 19 | 4 | 19 | 4 | 21 | 4 | 23 | ns |
| $t_{PHL}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | HFA, HFB | 1 | | 15 | 1 | 15 | 1 | 17 | 1 | 19 | ns |
| $t_{pd}$ | SAB or SBA¶ | B or A | 1 | | 11 | 1 | 11 | 1 | 13 | 1 | 15 | ns |
| $t_{pd}$ | A or B | B or A | 1 | | 11 | 1 | 11 | 1 | 13 | 1 | 15 | ns |
| $t_{pd}$ | LDCK↑, LDCKB↑ | AF/AEA, AF/AEB | 2 | | 19 | 2 | 19 | 2 | 21 | 2 | 23 | ns |
| $t_{pd}$ | UNCKA↑, UNCKB↑ | AF/AEA, AF/AEB | 2 | | 19 | 2 | 19 | 2 | 23 | 2 | 23 | ns |
| $t_{en}$ | DIR, $\overline{OE}$ | A or B | 2 | | 12 | 2 | 12 | 2 | 14 | 2 | 16 | ns |
| $t_{dis}$ | DIR, $\overline{OE}$ | A or B | 1 | | 10 | 1 | 10 | 1 | 12 | 1 | 14 | ns |

¶ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per 1 Kbits | Outputs enabled | $C_L$ = 50 pF, f = 5 MHz | 71 | pF |
| | | Outputs disabled | | 57 | |

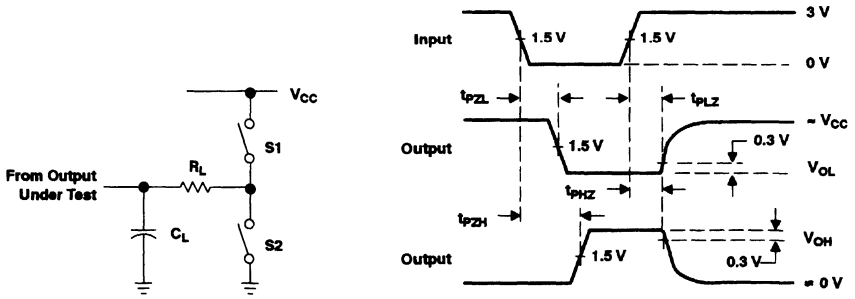
## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT

TOTEM-POLE OUTPUTS

**Figure 1. Standard CMOS Outputs (All Flags)**




LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

| PARAMETER | | $R_L$ | $C_L$† | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | – | 50 pF | Open | Open |

† Includes probe and test fixture capacitance.

**Figure 2. 3-State Outputs (A0–A8, B0–B8)**



TEXAS INSTRUMENTS

## TYPICAL CHARACTERISTICS

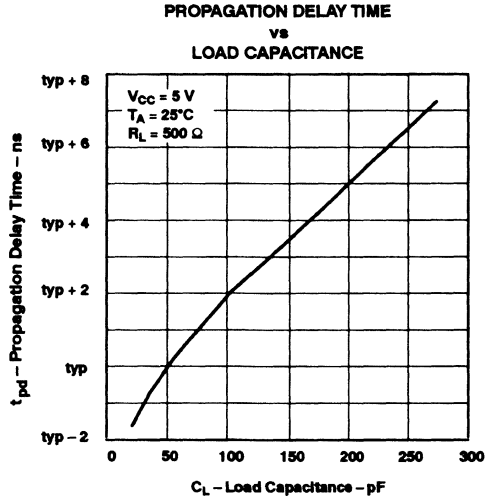



Figure 3

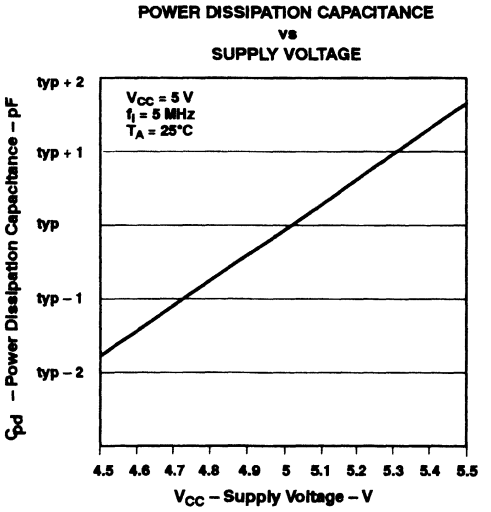



Figure 4

### calculating power dissipation

With $I_{CCF}$ taken from Figure 4, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

$I_{CC}$ = power-down $I_{CC}$ maximum
N = number of inputs driven by a TTL device
$\Delta I_{CC}$ = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
$C_{pd}$ = power dissipation capacitance
$C_L$ = output capacitive load
$f_i$ = data input frequency
$f_o$ = data output frequency

- **Independent Asynchronous Inputs and Outputs**
- **Bidirectional**
- **32 Words by 9 Bits Each**
- **Programmable Depth**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 22 ns Typ**
- **3-State Outputs**

## description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It consists of two FIFOs organized as 32 words by 9 bits each.

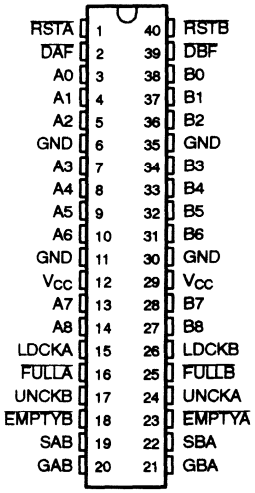
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

The SN74ALS2238 consists of bus transceiver circuits, two 32 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enables GAB and GBA are provided to control the transceiver functions. The SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low level selects real-time data and a high selects stored data. Eight fundamental bus-management functions can be performed as shown on the operating modes page.

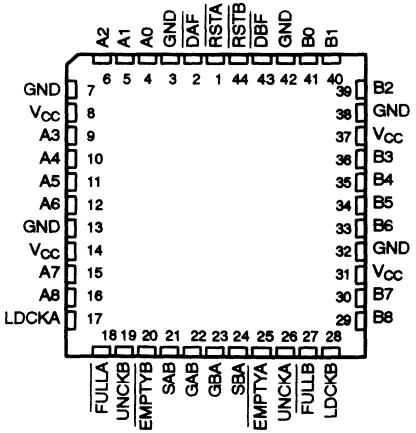
Data on the A or B data bus, or both, is written into the FIFOs on a low-to-high transition at the load clock input (LDCKA or LDCKB) and is read out on a low-to-high transition at the unload clock input (UNCKA or UNCKB). The memory is full when the number of words clocked in exceeds, by the defined depth, the number of words clocked out.

When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

**N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




IMPACT-X is a trademark of Texas Instruments Incorporated.

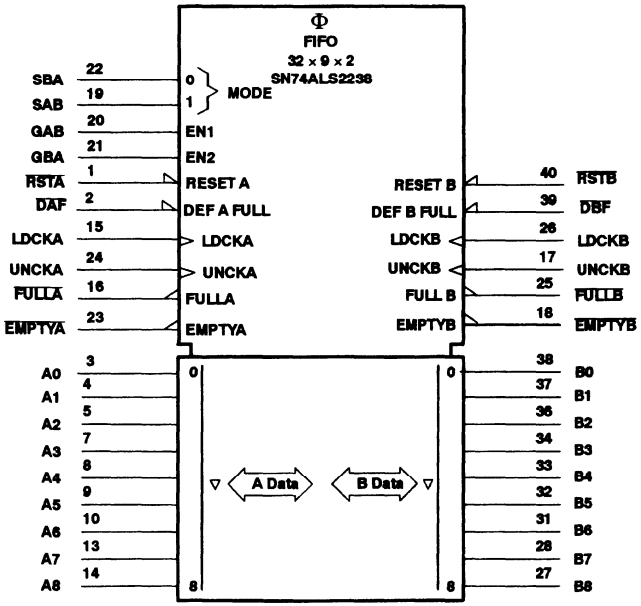
## description (continued)

Status of the FIFO memories is monitored by the $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, $\overline{\text{EMPTYA}}$, and $\overline{\text{EMPTYB}}$ output flags. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ are definable full flags. A high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0 through A4 into a register for use as the value of X. A high-to-low transition on $\overline{\text{DBF}}$ stores the binary value of B0 through B4 into a register for use as the value of Y. In this way, the depth of either FIFO can be defined to be one to thirty-two words deep. The value of X and Y must be defined after power up or the stored value of X and Y will be ambiguous. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ outputs are low when their corresponding memories are full and high when the memories are not full.

The $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ outputs are low when their corresponding memories are empty and high when they are not empty. The status flag outputs are always active.

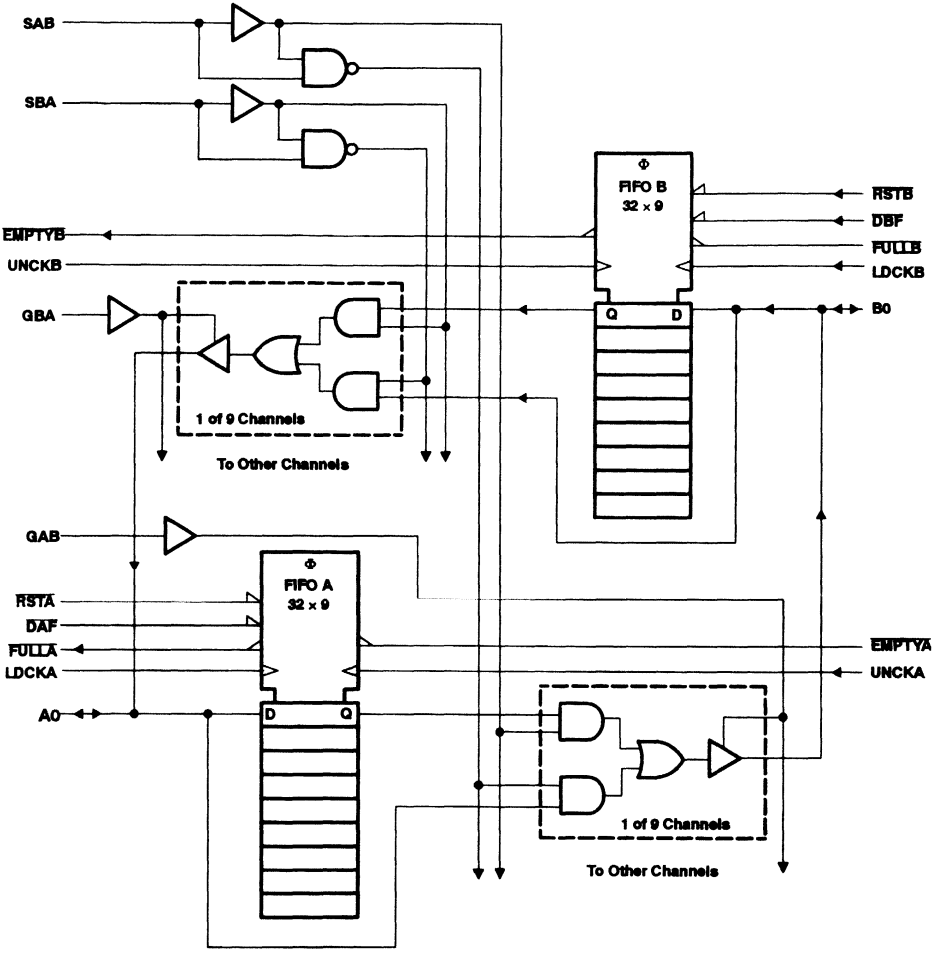
A low-level pulse on the $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inputs resets the control pointers on FIFO A or FIFO B and also sets $\overline{\text{EMPTYA}}$ low and $\overline{\text{FULLA}}$ high or $\overline{\text{EMPTYB}}$ low and $\overline{\text{FULLB}}$ high. The outputs are not reset to any specific logic levels. With $\overline{\text{DAF}}$ at a low level, a low-level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 minus X, where X is the value stored above. With $\overline{\text{DAF}}$ at a high level, a low level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 words. The depth of FIFO B is set in a similar manner. The first low-to-high transition on LDCKA or LDCKB, either after a reset pulse or from an empty condition, will cause $\overline{\text{EMPTYA}}$ or $\overline{\text{EMPTYB}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

## logic symbol†

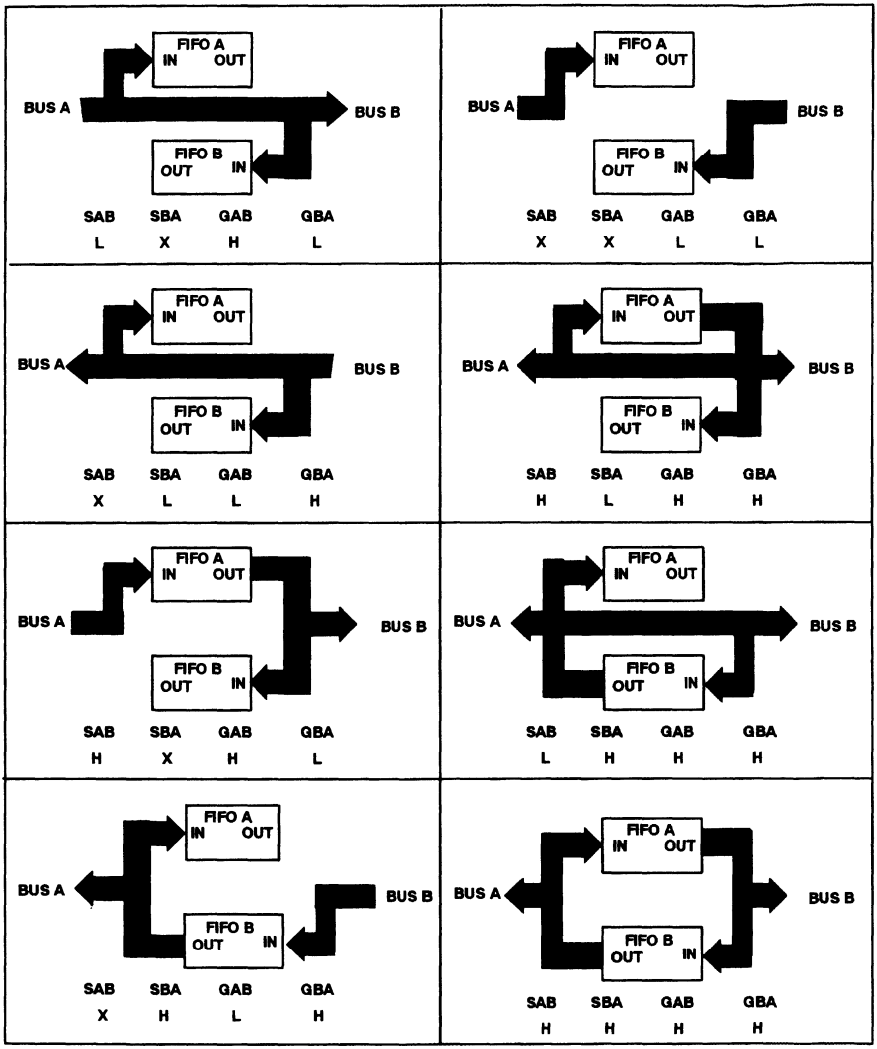



† This symbol is in accordance with ANSI/IEEE Std 91-1984.
Pin numbers shown are for the N package.

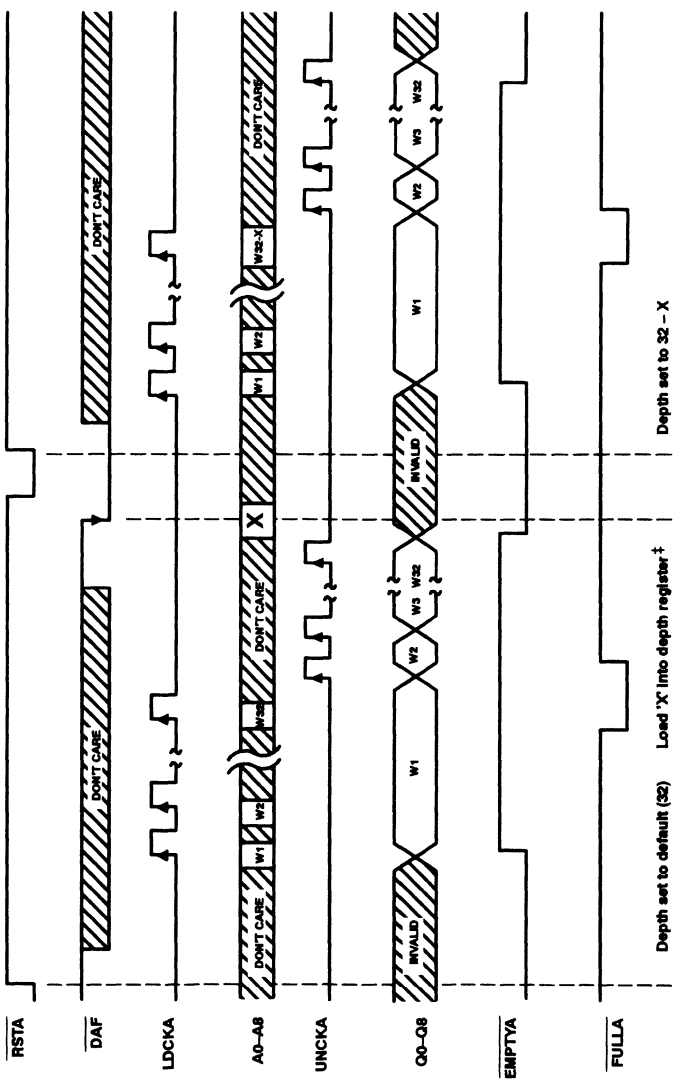
## logic diagram (positive logic)



## operating modes



## timing diagram




† Operation of FIFO B is the same as shown above.
‡ X includes A0 through A4 only. A5 through A8 are ignored.

SELECT-MODE CONTROL TABLE

| CONTROL | | OPERATION | |
|---|---|---|---|
| SAB | SBA | A BUS | B BUS |
| L | L | Real-time B to A bus | Real-time A to B bus |
| L | H | FIFO B to A bus | Real-time A to B bus |
| H | L | Real-time B to A bus | FIFO A to B bus |
| H | H | FIFO B to A bus | FIFO A to B bus |

OUTPUT-ENABLE CONTROL TABLE

| CONTROL | | OPERATION | |
|---|---|---|---|
| GAB | GBA | A BUS | B BUS |
| H | H | A bus enabled | B bus enabled |
| L | H | A bus enabled | Isolation/input to B bus |
| H | L | Isolation/input to A bus | B bus enabled |
| L | L | Isolation/input to A bus | Isolation/input to B bus |

## programming procedure for depth of FIFO A†

Program:

Step 1. With $\overline{RSTA}$ at a high level, take $\overline{DAF}$ from a high level to a low level. The high-to-low transition on $\overline{DAF}$ stores the binary value of A0-A4 for use as the value of 'X' in defining the depth of FIFO A.

Step 2. With $\overline{DAF}$ held low, pulse the $\overline{RSTA}$ signal low. On the low-to-high transition of $\overline{RSTA}$, FIFO A is set to a depth of 32 minus 'X', where X is the value of A0-A4 stored above.

Step 3. To redefine the depth of FIFO A to 32 words, hold $\overline{DAF}$ at a high level and pulse the $\overline{RSTA}$ signal low.

† The programming procedures used to define the depth of FIFO B are the same as the procedure above.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage: Control inputs ..... 7 V
I/O ports ..... 5.5 V
Voltage applied to a diabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Maximum junction temperature ..... 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | A or B ports | | | −15 | mA |
| | | Status flags | | | −0.4 | |
| $I_{OL}$ | Low-level output current | A or B ports | | | 24 | mA |
| | | Status flags | | | 8 | |
| $f_{clock}$ | Clock frequency | LDCKA or LDCKB | 0 | | 40 | MHz |
| | | UNCKA or UNCKB | 0 | | 40 | |
| $t_w$ | Pulse duration | $\overline{RSTA}$ or $\overline{RSTB}$ low | 17 | | | ns |
| | | LDCKA or LDCKB low | 12.5 | | | |
| | | LDCKA or LDCKB high | 10 | | | |
| | | UNCKA or UNCKB low | 12.5 | | | |
| | | UNCKA or UNCKB high | 10 | | | |
| | | $\overline{DAF}$ or $\overline{DBF}$ high | 10 | | | |
| $t_{su}$ | Setup time | Data before LDCKA or LDCKB↑ | 7 | | | ns |
| | | Define depth: D4-D0 before $\overline{DAF}$ or $\overline{DBF}$↓ | 6 | | | |
| | | Define depth: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 45 | | | |
| | | Define depth (32): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 32 | | | |
| | | LDCKA or LDCKB (inactive) before $\overline{RSTA}$ or $\overline{RSTB}$↑ | 5 | | | |
| $t_h$ | Hold time | Data after LDCKA or LDCKB↑ | 3 | | | ns |
| | | Define depth: D4-D0 after $\overline{DAF}$ or $\overline{DBF}$↓ | 4 | | | |
| | | Define depth: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | | |
| | | Define depth (32): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 0 | | | |
| | | LDCKA or LDCKB (inactive) after $\overline{RSTA}$ or $\overline{RSTB}$↑ | 5 | | | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCKA or LDCKB and UNCKA or UNCKB clock inputs. Any excessive noise or glitching on the clock inputs (which violates the $V_{IL}$, $V_{IH}$, or minimum pulse duration limits) can cause a false clock or improper operation of the internal read and write pointers.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | Status flags | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | V |
| | A or B ports | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$−2 | | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −3 mA | 2.4 | 3.2 | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −15 mA | 2 | | | |
| $V_{OL}$ | A or B ports | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | Status flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_I$ | $\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| | A or B ports | | | | | 0.2 | |
| $I_{IH}$ | $\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| | A or B ports‡ | | | | | 40 | |
| $I_{IL}$ | $\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LCKA, LDCKB, UNCKA, UNCKB | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | mA |
| | A or B ports‡ | | | | | −0.4 | |
| $I_O$§ | A or B ports‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −20 | | −130 | mA |
| | Status flags | | | −15 | | −100 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 190 | 350 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the offstate output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | |
| $f_{max}$ | LDCK, UNCK | | 40 | | | MHz |
| $t_{pd}$ | LDCKA↑, LDCKB↑ | B/A | 7 | 22 | 33 | ns |
| | UNCKA↑, UNCKB↑ | | 7 | 20 | 29 | |
| $t_{PLH}$ | LDCKA↑, LDCKB↑ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 5 | 12 | 22 | ns |
| $t_{PHL}$ | UNCKA↑, UNCKB↑ | | 5 | 12 | 22 | |
| $t_{PHL}$ | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | $\overline{EMPTYA}$, $\overline{EMPTYB}$ | 5 | 12 | 22 | ns |
| $t_{PHL}$ | LDCKA↑, LDCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 5 | 12 | 22 | ns |
| $t_{PLH}$ | UNCKA↑, UNCKB↑ | $\overline{FULLA}$, $\overline{FULLB}$ | 5 | 12 | 23 | ns |
| | $\overline{RSTA}$↓, $\overline{RSTB}$↓ | | 6 | 15 | 28 | |
| $t_{pd}$ | SAB/SBA‡ | B/A | 2 | 11 | 18 | ns |
| | A/B | | 2 | 8 | 15 | |
| $t_{en}$ | GBA/GAB | A/B | 2 | 6 | 15 | ns |
| $t_{dis}$ | GBA/GAB | A/B | 1 | 5 | 12 | ns |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *LSI Logic Data Book*, 1986.

- **Free-Running CLKA and CLKB May Be Asynchronous or Coincident**
- **Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Dynamic Port B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte Order Swapping on Port B**
- **Almost Full and Almost Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{\text{EFA}}$, FFA, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **$\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BICMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in 132-Pin Quad Flatpack (PQ) or Space-Saving 120-Pin Shrink Quad Flatpack (PCB)**

## description

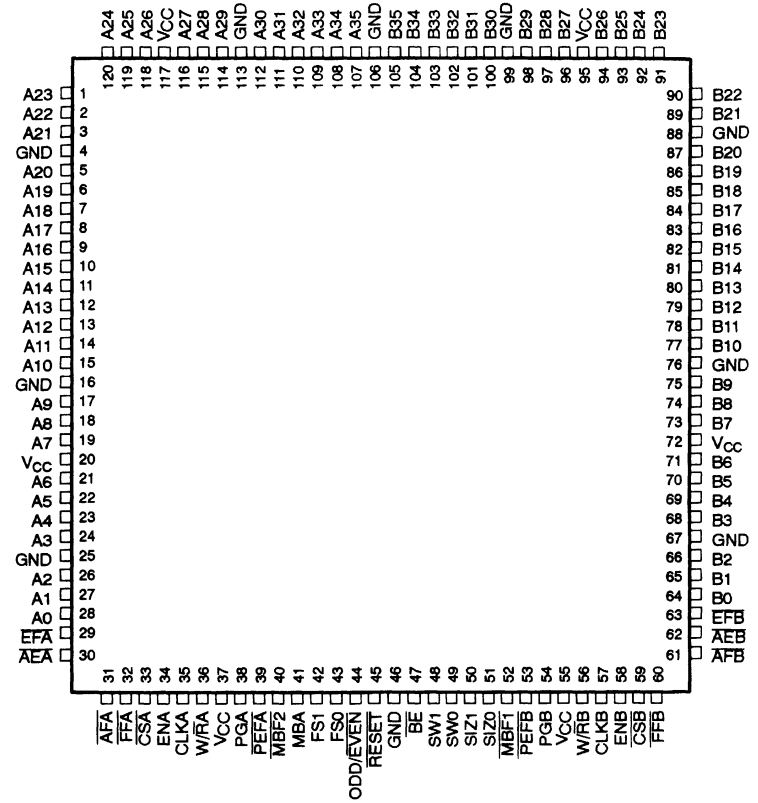
The SN74ABT7815 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. Two independent 64 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. FIFO data on port B may be input and output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte order swapping are possible with any bus size selection. Communication between each port may bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port.

The SN74ABT7815 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses controlled by a synchronous interface.

The full flag and almost full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag and almost empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

PRODUCT PREVIEW

PCB PACKAGE
(TOP VIEW)

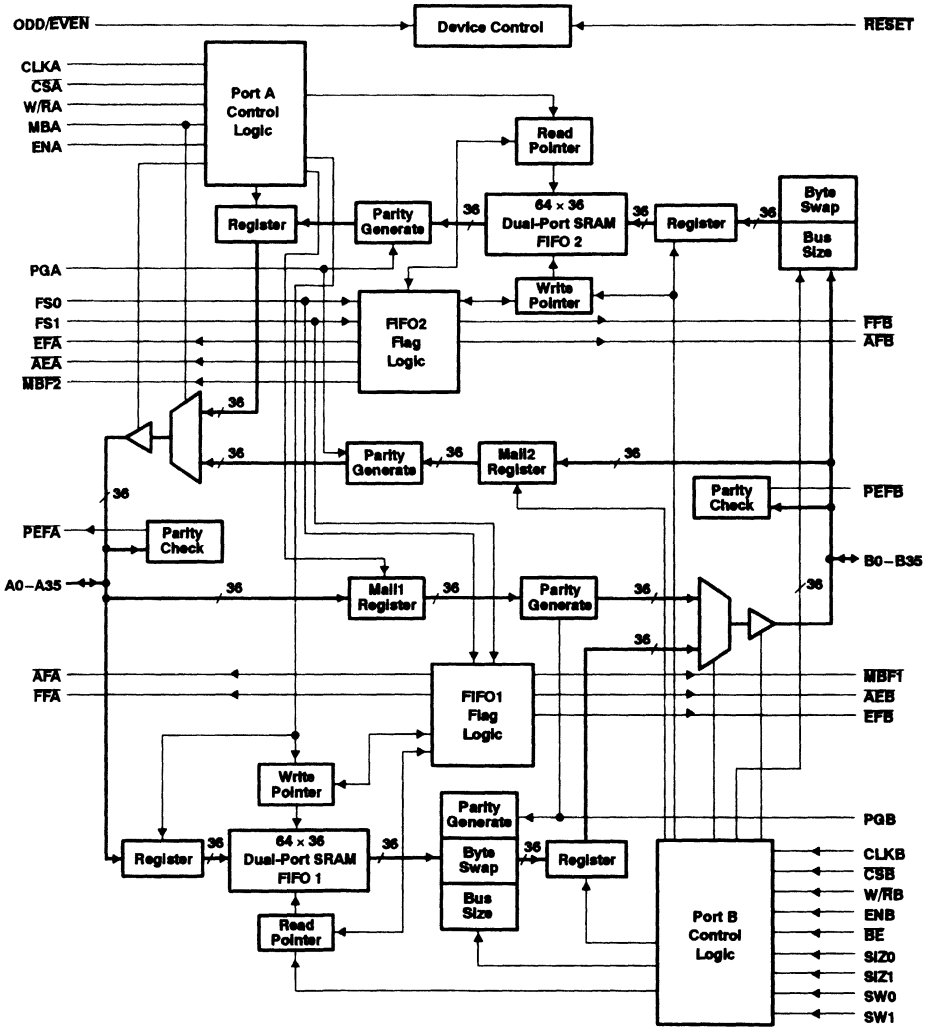



PRODUCT PREVIEW



TEXAS INSTRUMENTS

## functional block diagram




PRODUCT PREVIEW

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A35 | I/O | Port A data. 36-bit bidirectional data port for side A. |
| $\overline{AEA}$ | O | FIFO2 almost empty flag. $\overline{AEA}$ is synchronous to CLKA and is low when the number of 36-bit long words in FIFO2 is less than or equal to the selected offset value. |
| $\overline{AEB}$ | O | FIFO1 almost empty flag. $\overline{AEB}$ is synchronous to CLKB and is low when the number of 36-bit long words in FIFO1 is less than or equal to the selected offset value. |
| $\overline{AFA}$ | O | FIFO1 almost full flag. $\overline{AFA}$ is synchronous to CLKA and is low when the number of 36-bit empty locations in FIFO1 is less than or equal to the selected offset value. |
| $\overline{AFB}$ | O | FIFO2 almost full flag. $\overline{AFB}$ is synchronous to CLKB and is low when the number of 36-bit empty locations in FIFO2 is less than or equal to the selected offset value. |
| B0–B35 | I/O | Port B data. 36-bit bidirectional data port for side B. |
| $\overline{BE}$ | I | Big-endian select. Selects the bytes on port B for use with byte or word data transfers. A low on $\overline{BE}$ selects the most significant bytes of B0–B35 for use, and a high selects the least significant bytes. |
| CLKA | I | Port A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and may be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are all synchronous to the low-to-high transition of CLKA. |
| CLKB | I | Port B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and may be asynchronous or coincident to CLKA. Port B byte swapping and data port sizing operations are also synchronous to the low-to-high transition of CLKB. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronous to the low-to-high transition of CLKB. |
| $\overline{CSA}$ | I | Port A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high. |
| $\overline{CSB}$ | I | Port B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high. |
| $\overline{EFA}$ | O | FIFO2 empty flag. $\overline{EFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{EFA}$ is low, FIFO2 is empty, and reads are disabled. $\overline{EFA}$ is forced low when FIFO2 is reset and goes high on the second low-to-high transition of CLKA after data is loaded to empty memory. |
| $\overline{EFB}$ | O | FIFO1 empty flag. $\overline{EFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EFB}$ is low, FIFO1 is empty, and reads are disabled. $\overline{EFB}$ is forced low when FIFO1 is reset and goes high on the second low-to-high transition of CLKB after data is loaded to empty memory. |
| ENA | I | Port A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A. |
| ENB | I | Port B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B. |
| $\overline{FFA}$ | O | FIFO1 full flag. $\overline{FFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FFA}$ is low, FIFO1 is full, and writes to its array are disabled. $\overline{FFA}$ goes low when FIFO1 is reset and goes high on the second low-to-high transition of CLKA after reset. |
| $\overline{FFB}$ | O | FIFO2 full flag. $\overline{FFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{FFB}$ is low, FIFO2 is full, and writes to its array are disabled. $\overline{FFB}$ goes low when FIFO2 is reset and goes high on the second low-to-high transition of CLKB after reset. |
| FS0, FS1 | I | Flag offset selects. The low-to-high transition of $\overline{RESET}$ latches the value of the FS0 and FS1, which selects one of four preset values for the almost empty and almost full offsets. |
| MBA | I | Port A mailbox select. A high level chooses a mailbox register for a port A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output, and a low level selects FIFO2 data for output. |
| $\overline{MBF1}$ | O | Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set back high by a low-to-high transition of CLKB when a port B read is selected and both SIZ1 and SIZ0 are high. $\overline{MBF1}$ is set high when FIFO1 is reset. |
| $\overline{MBF2}$ | O | Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set back high by a low-to-high transition of CLKA when a port A read is selected and MBA is high. $\overline{MBF2}$ is set high when FIFO2 is reset. |
| ODD/$\overline{EVEN}$ | I | Odd/$\overline{even}$ parity select. Odd parity is checked on each port when ODD/$\overline{EVEN}$ is high, and even parity is checked when ODD/$\overline{EVEN}$ is low. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for read operations. |

**Terminal Functions (continued)**

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| PEFA | O | Port A parity error flag. When any byte on A0–A35 fails parity, $\overline{PEFA}$ is forced low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the level on the ODD/$\overline{EVEN}$ select input. |
| PEFB | O | Port B parity error flag. When any valid byte on B0–B35 fails parity, $\overline{PEFB}$ is forced low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used in the bus size selection for port B. The type of parity checked is determined by the level on the ODD/$\overline{EVEN}$ select input. |
| PGA | I | Port A parity generation. A high on PGA selects parity to be generated for data read from port A. The level on the ODD/$\overline{EVEN}$ parity select input determines the type of parity generated. |
| PGB | I | Port B parity generation. A high on PGB selects parity to be generated for data read from port B. The level on the ODD/$\overline{EVEN}$ parity select input determines the type of parity generated. |
| $\overline{RESET}$ | I | Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RESET}$ is low. This sets the $\overline{AFA}$ and $\overline{AFB}$ flags high and the $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, $\overline{AEB}$, $\overline{FFA}$, and $\overline{FFB}$ flags low. The low-to-high transition of $\overline{RESET}$ latches the status of FS1 and FS0 for almost full and almost empty offset selection. |
| SIZ0, SIZ1 | I | Port B bus size selects. A low-to-high transition of CLKB latches the value of SIZ0, SIZ1, and $\overline{BE}$ for a bus size select, and the following low-to-high transition of CLKB implements the latched value as a port B bus size. Port B bus sizes may be selected from long word, word, and byte. A high on both SIZ1 and SIZ0 directs a write or read on port B to a mailbox register. |
| SW0, SW1 | I | Port B byte swap selects. At the beginning of each long word transfer, one of four modes of byte order swapping is selected by SW0 and SW1. The four modes of byte order swapping are no swap, byte swap, word swap, and byte-word swap. Byte order swapping is possible with any bus size selection. |
| W/$\overline{RA}$ | I | Port A write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high. |
| W/$\overline{RB}$ | I | Port B write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{RB}$ is high. |

## FIFO function

The state of the A0–A35 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to FIFO1 from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, MBA is low, ENA is high, and the $\overline{FFA}$ flag is high. Data is read from FIFO2 to the A0–A35 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, MBA is low, ENA is high, and the $\overline{EFA}$ flag is high.

The state of the B0–B35 outputs is controlled by $\overline{CSB}$ and W/$\overline{RB}$. When both $\overline{CSB}$ and W/$\overline{RB}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. Data is written to FIFO2 from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is high, ENB is high, the $\overline{FFB}$ flag is high, and either SIZ0 or SIZ1 is low. Data is read from FIFO1 to the port B outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, ENB is high, the $\overline{EFB}$ flag is high, and either SIZ0 or SIZ1 is low.

The setup and hold time constraints to the port clocks for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are for enabling write and read operations and are not related to high-impedance control of the data outputs. If the master enable signal for a port (ENA or ENB) is set low during a clock cycle, the chip select and write/read select may switch at any time during the cycle to change the state of the data outputs.

Each FIFO flag is two-stage synchronized to a port clock for use as a reliable synchronous control signal. CLKA synchronizes the status of the empty flag ($\overline{EFA}$) and almost empty flag ($\overline{AEA}$) of FIFO2 and the full flag ($\overline{FFA}$) and almost full flag ($\overline{AFA}$) of FIFO1. CLKB synchronizes the status of the empty flag ($\overline{EFB}$) and almost empty flag ($\overline{AEB}$) of FIFO1 and the full flag ($\overline{FFB}$) and almost full flag ($\overline{AFB}$) of FIFO2.

### FIFO function (continued)

When the full flag ($\overline{FFA}$, $\overline{FFB}$) of a port is low, the FIFO receiving input from the port is full, and writes are disabled to its array. When the empty flag ($\overline{EFA}$, $\overline{EFB}$) of a port is low, the FIFO that outputs data to the port is empty, and reads from its memory are disabled.

### mailbox registers

A 36-bit data word may be exchanged between ports and circumvent the normal FIFO path. The mailbox select input (MBA) chooses between a mail register and a FIFO for a port A data transfer operation. Port B accesses a mail register when the bus size select inputs (SIZ0, SIZ1) are both high. A0–A35 data is written to the mail1 register on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is high, ENA is high, and MBA is high. B0–B35 data is written to the mail2 register on a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{R}$B is high, ENB is high, and both SIZ0 and SIZ1 are high.

When data is written to a mail register, its mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) is set low. The $\overline{MBF1}$ flag is set high on a low-to-high transition of CLKB when a read is selected for port B and both SIZ0 and SIZ1 are high. The $\overline{MBF2}$ flag is set high on a low-to-high transition of CLKA when a read is selected for port A and the MBA input is high. The data in a mailbox register remains intact after it is read and changes only when new data is written to the register. When the B0–B35 outputs are active, mail1 data is output if both SIZ0 and SIZ1 are high, and FIFO1 data is output if either bus size input is low. The level on MBA selects between FIFO2 and mail2 data for output on A0–A35.

### reset

The SN74ABT7815 is reset by taking the reset input ($\overline{RESET}$) low for at least four CLKA and four CLKB low-to-high transitions. This resets the internal read and write pointers of each FIFO to their initial locations and forces $\overline{AFA}$ and $\overline{AFB}$ flags high and $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, $\overline{FFB}$, $\overline{AEA}$, and $\overline{AEB}$ flags low. The reset input may by asynchronous with respect to either clock. Resetting the device also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. Data outputs of the FIFO and mailbox register are not reset to any specific logic level. The device must be reset upon power up.

### almost full and almost empty flags

Four preset values are available for the offsets of the almost full and almost empty flags of the SN74ABT7815. The flag select inputs (FS0, FS1) are sampled by the low-to-high transition of the reset input ($\overline{RESET}$), and the offsets for $\overline{AFA}$, $\overline{AEA}$, $\overline{AFB}$, and $\overline{AEB}$ are set according to the flag programming table.

An almost empty flag is low when the number of 36-bit words stored in its FIFO is less than or equal to the flag's offset value. An almost full flag is low when the number of empty locations left in its FIFO is less than or equal to the flag's offset value. Data in the output register of a FIFO has been read from memory, and its previous location is free.

**FLAG PROGRAMMING TABLE**

| FS1 | FS0 | RESET | $\overline{AF}$ AND $\overline{AE}$ OFFSET |
|---|---|---|---|
| H | H | ↑ | 16 |
| H | L | ↑ | 12 |
| L | H | ↑ | 8 |
| L | L | ↑ | 4 |

PRODUCT PREVIEW

### dynamic bus sizing

Port B may be configured in a 36-bit long-word, 18-bit-word, or 9-bit-byte bus size with a choice of big- or little-endian formats to read data from FIFO1 or input data to FIFO2. The bus size can be changed synchronous to CLKB to accommodate peripherals of various bus sizes.

A bus size is selected on the low-to-high transition of CLKB by the levels on the bus size inputs (SIZ0, SIZ1) and the big-endian input ($\overline{BE}$) according to Figure 1. The bus size is implemented on port B by the following low-to-high transition of CLKB. When reading data from FIFO1 and a bus size of word or byte length is implemented for port B, the unused outputs of B0–B35 remain active but static, holding the last data value to decrease power consumption.

The port B almost empty flag ($\overline{AEB}$) and almost full flag ($\overline{AFB}$) always measure the number of 36-bit memory locations in the FIFOs regardless of the bus size. The port B empty flag ($\overline{EFB}$) and full flag ($\overline{FFB}$) are based on the bus size selection.

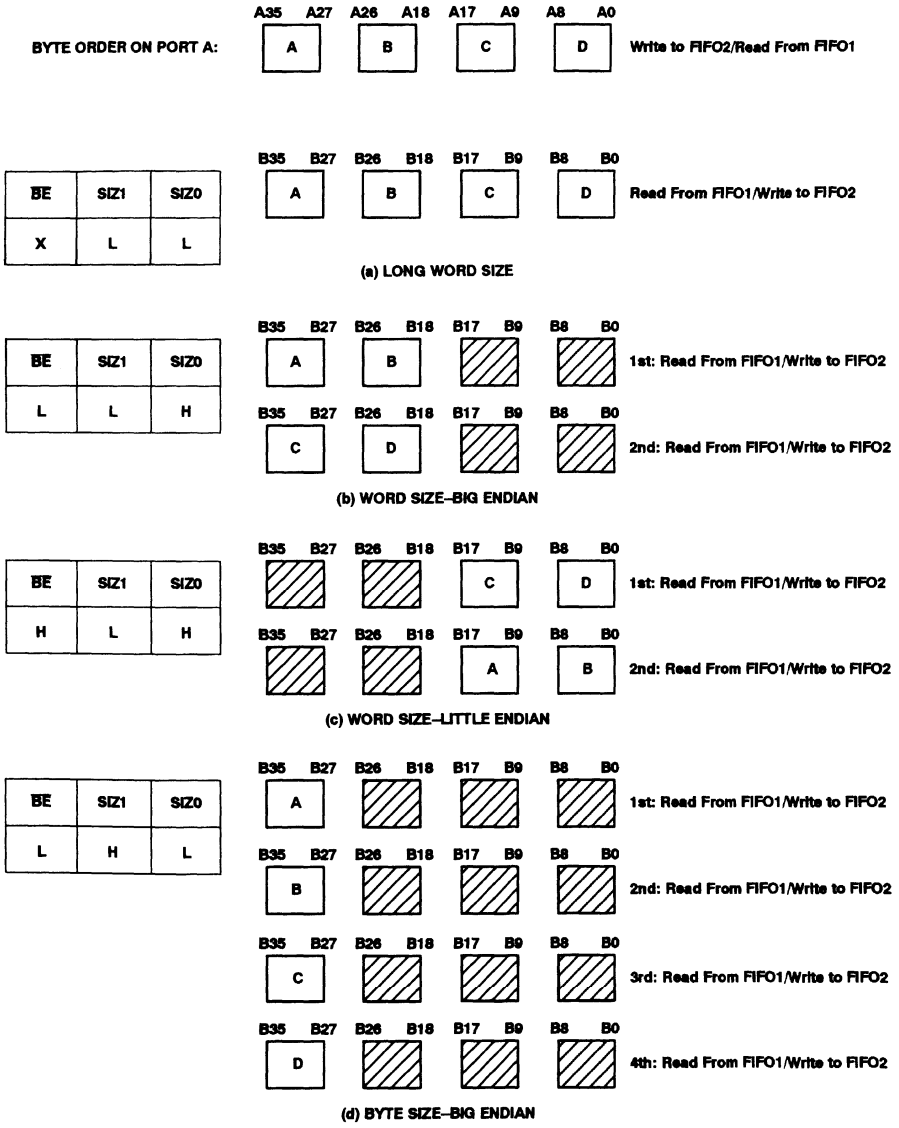
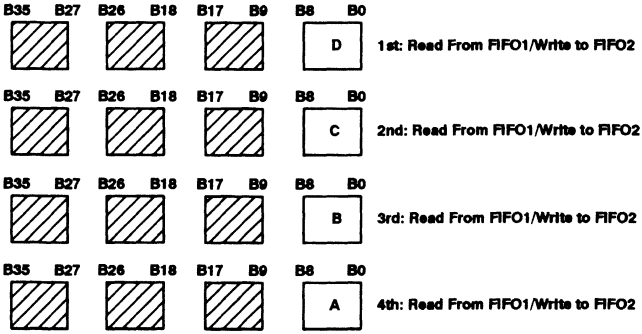



**Figure 1. Dynamic Bus Sizing**

| BE | SIZ1 | SIZ0 |
|---|---|---|
| H | H | L |




(e) BYTE SIZE–LITTLE ENDIAN

**Figure 1. Dynamic Bus Sizing (continued)**

### byte swapping

The byte order of port B can be changed synchronous to CLKB for FIFO data passing through port B. Four modes of byte order swapping (including no swap) can be done with any data port size selection. The order of the bytes can be rearranged, but the bit order within the bytes remains constant.

When reading data from FIFO1 to port B, the byte arrangement is chosen by the swap inputs (SW0, SW1) on a low-to-high transition of CLKB that reads a new long word from FIFO1. Data is unloaded to the data outputs according to Figure 2.

When writing data from port B to FIFO2, the byte arrangement is chosen by the swap inputs (SW0, SW1) on a low-to-high transition of CLKB that writes a new long word to FIFO2. Data is loaded to memory according to Figure 2. The status of the SW0 and SW1 inputs has no effect when a port B read or write operation accesses a bypass register.

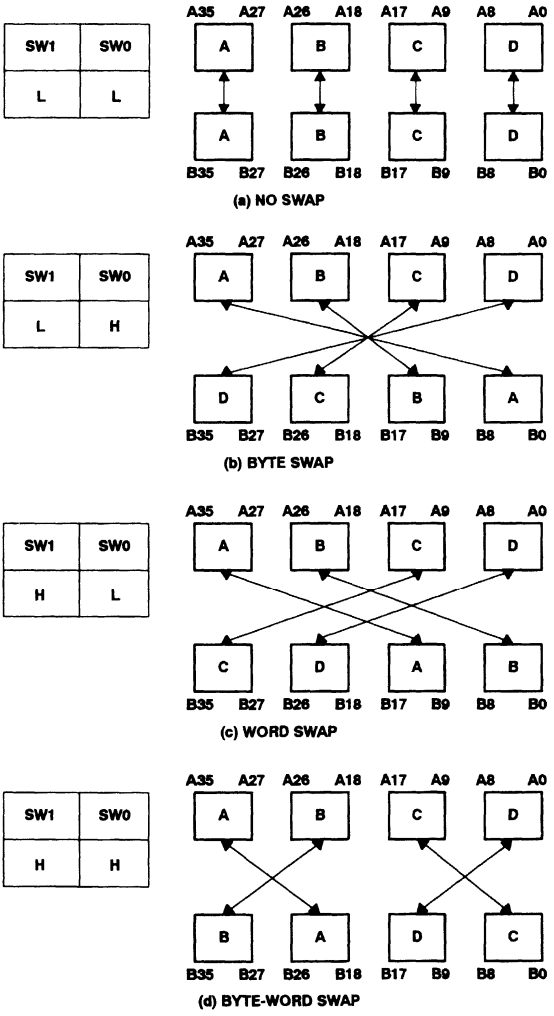



**Figure 2. Byte Swapping (Long Word Size Example)**

### parity checking and parity generation

The parity error flag for port A ($\overline{PEFA}$) is low if any byte on A0–A35 fails a parity check. The bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. The bytes on port B are also arranged as B0–B8, B9–B17, B18–B26, and B27–B35 with the most signicant bit of each byte used for parity. Only the port B bytes selected by the bus sizing inputs ($\overline{BE}$, SIZ1, SIZ0) are checked for parity, with a parity failure of any of the selected bytes forcing a low on the port B parity error flag ($\overline{PEFB}$). The odd/$\overline{even}$ select input (ODD/$\overline{EVEN}$) chooses the type of parity checked on both port A and port B.

Parity can be generated for data read from a port by asserting the port's parity generation input (PGA, PGB) for the low-to-high transition of the clock that reads the data to the output. When parity generation is selected for a port read, parity is generated for each byte based on the ODD/$\overline{EVEN}$ input selection and stored in the most significant bit of the byte. Parity can be generated for reads from FIFO memory and reads from the mailbox register.

### recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −4 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

PRODUCT PREVIEW

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 30 pF (unless otherwise noted)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7815-15 | | 'ACT7815-20 | | 'ACT7815-25 | | 'ACT7815-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKA or CLKB | | 67 | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | CLKA↑ | A0–A35 | | 10 | | 12 | | 14 | | 16 | ns |
| | CLKB↑ | B0–B35 | | 10 | | 12 | | 14 | | 16 | |
| | CLKA↑ | $\overline{EFA}$, $\overline{FFA}$, $\overline{AEA}$, $\overline{AFA}$ | | 10 | | 12 | | 14 | | 16 | |
| | CLKB↑ | $\overline{EFB}$, $\overline{FFB}$, $\overline{AEB}$, $\overline{AFB}$ | | 10 | | 12 | | 14 | | 16 | |
| $t_{pd}$ | MBA | A0–A35 | | 11 | | 12 | | 14 | | 16 | |
| | SIZ1, SIZ0† | B0–B35 | | 11 | | 12 | | 14 | | 16 | |
| $t_{pd}$‡ | MBA | A8, A17, A26, A35 | | 14 | | 15 | | 17 | | 19 | ns |
| | SIZ1, SIZ0 | B8, B17, B26, B35 | | 14 | | 15 | | 17 | | 19 | |
| $t_{PHL}$ | CLKA↑ | $\overline{MBF1}$ | | 10 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKB↑ | | | 9 | | 11 | | 13 | | 15 | |
| $t_{PHL}$ | CLKB↑ | $\overline{MBF2}$ | | 10 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKA↑ | | | 9 | | 11 | | 13 | | 15 | |
| $t_{pd}$ | A0–A35 | $\overline{PEFA}$ | | 13 | | 14 | | 16 | | 18 | ns |
| | B0–B35 | $\overline{PEFB}$ | | 13 | | 14 | | 16 | | 18 | |
| $t_{pd}$ | ODD/EVEN | $\overline{PEFA}$ | | 12 | | 13 | | 15 | | 17 | ns |
| | | $\overline{PEFB}$ | | 12 | | 13 | | 15 | | 17 | |
| $t_{PHL}$ | $\overline{RESET}$ | $\overline{AEA}$, $\overline{AEB}$ | | | | | | | | | ns |
| $t_{PLH}$ | $\overline{RESET}$ | $\overline{AFA}$, $\overline{AFB}$ | | | | | | | | | ns |
| | | $\overline{MBF1}$, $\overline{MBF2}$ | | | | | | | | | |
| $t_{en}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | | | | | | | | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | | | | | | | | | |
| $t_{dis}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | | | | | | | | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | | | | | | | | | |

† Selecting between FIFO1 and mail1 output with SIZ1 and SIZ0
‡ Parity generation is selected when reading a bypass register.

PRODUCT PREVIEW

SCBS129–JULY 1992

- Free-Running CLKA and CLKB May Be Asynchronous or Coincident
- Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions
- Almost Full/Almost Empty Flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{AEA}$ and $\overline{AFA}$ Synchronized to CLKA
- IRB, ORB, $\overline{AEB}$ and $\overline{AFB}$ Synchronized to CLKB
- Passive Parity Checking on Each Port
- Parity Generation Can Be Selected for Each Port
- Low-Power Advanced BiCMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Available in 132-pin Quad Flat Package (PQ) or Space-Saving 120-pin Shrink Quad Flat Package (PCB)

## description

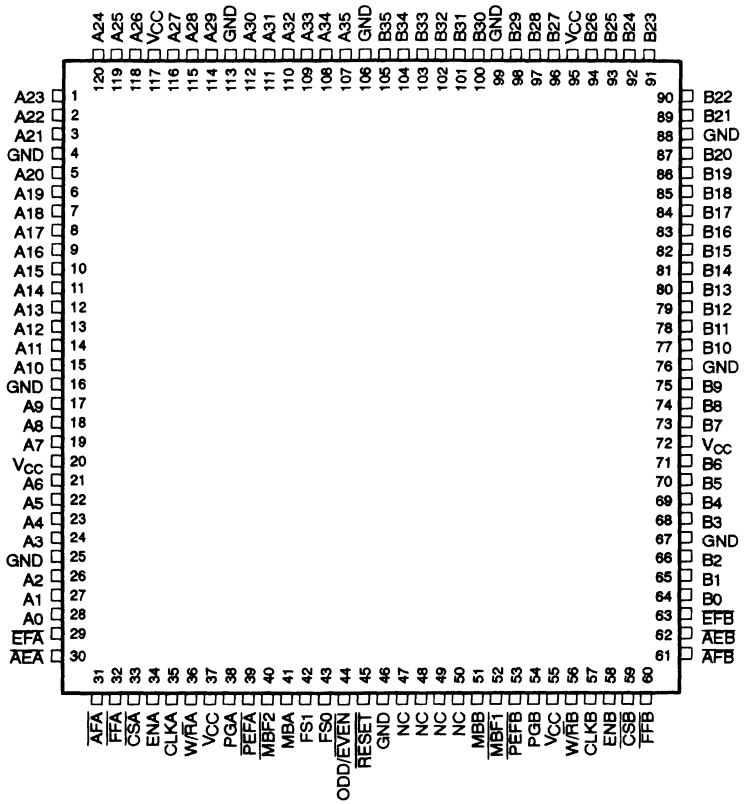
The SN74ABT7816 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 11 ns. Two independent 64 x 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port may bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if it is not desired. Parity generation can be selected for the data read from each port.

The SN74ABT7816 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input ready flag and almost full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output ready flag and almost empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

PRODUCT PREVIEW

PCB PACKAGE
(TOP VIEW)




NC–No internal connection

PRODUCT PREVIEW



TEXAS INSTRUMENTS

- **Member of the Texas Instruments *Widebus+*™ Family**
- **Free-Running CLKA and CLKB May Be Asynchronous or Coincident**
- **64 × 36 Clocked FIFO Buffering Data From Port A to Port B**
- **Mailbox Register in Each Direction**
- **Dynamic Port B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte Order Swapping on Port B**
- **Almost Full and Almost Empty Flags**
- **Microprocessor Interface Control Logic**
- **FF and $\overline{AF}$ Flags Synchronized by CLKA**
- **EF and $\overline{AE}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BICMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 11 ns**
- **Available in 132-Pin Quad Flat Package (PQ) or Space-Saving 120-Pin Shrink Quad Flat Package (PCB)**

## description

The SN74ABT7817 is a high-speed, low-power BiCMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 11 ns. The 64 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. FIFO data on port B may be output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte order swapping are possible with any bus size selection. Communication between each port may take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port.

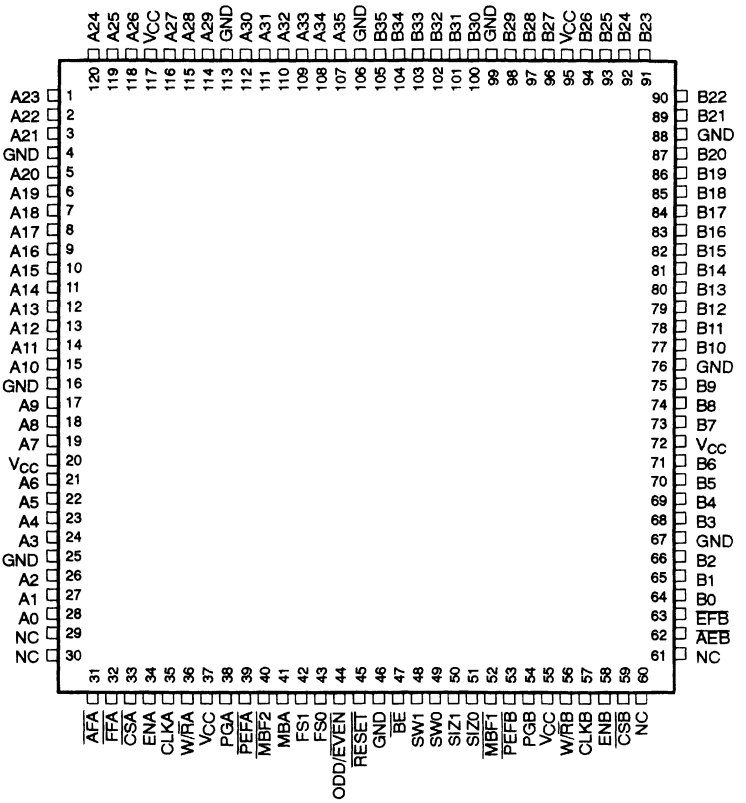
The SN74ABT7817 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The full flag ($\overline{FF}$) and almost full flag ($\overline{AF}$) of the FIFO are two-stage synchronized to CLKA. The empty flag ($\overline{EF}$) and almost empty flag ($\overline{AE}$) of the FIFO are two-stage synchronized to CLKB.

PRODUCT PREVIEW

Widebus+ is a trademark of Texas Instruments Incorporated.

PCB PACKAGE
(TOP VIEW)




NC–No internal connection

PRODUCT PREVIEW



TEXAS INSTRUMENTS

- **Free-Running CLKA and CLKB May Be Asynchronous or Coincident**
- **64 × 36 Clocked FIFO Buffering Data From Port A to Port B**
- **Almost Full and Almost Empty Flags**
- **Microprocessor Interface Control**
- **IR and $\overline{AF}$ Flags Synchronized to CLKA**
- **OR and $\overline{AE}$ Flags Synchronized to CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 11 ns**
- **Available in 132-Pin Quad Flat Package (PQ) or Space-Saving 120-Pin Shrink Quad Flat Package (PCB)**

## description

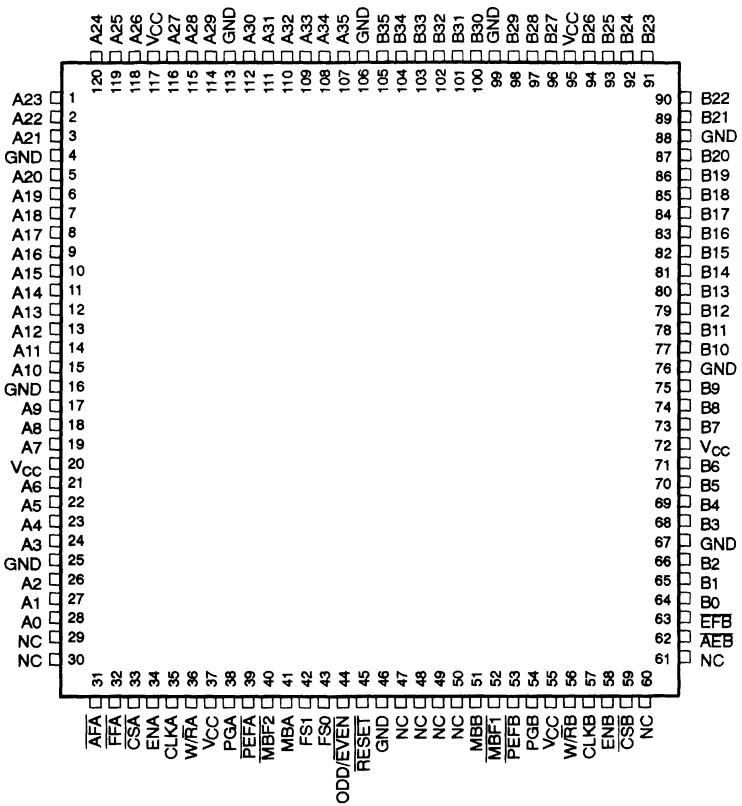
The SN74ABT7818 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 11 ns. The 64 x 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions and two flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port may take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if it is not desired. Parity generation can be selected for the data read from each port.

The SN74ABT7818 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input ready flag (IR) and almost full flag ($\overline{AF}$) of the FIFO are two-stage synchronized to CLKA. The output ready flag (OR) and almost empty flag ($\overline{AE}$) of the FIFO are two-stage synchronized to CLKB.

PRODUCT PREVIEW

PCB PACKAGE
(TOP VIEW)




NC–No internal connection

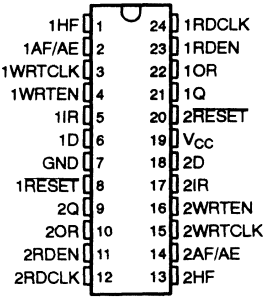
PRODUCT PREVIEW



TEXAS INSTRUMENTS

- **Dual Independent FIFOs Organized As:**
  - **64 Words by 1 Bit Each – SN74ACT2226**
  - **256 Words by 1 Bit Each – SN74ACT2228**
- **Free-Running Read and Write Clocks May Be Asynchronous or Coincident on Each FIFO**
- **Input Ready Flags Synchronized to Write Clocks**
- **Output Ready Flags Synchronized to Read Clocks**
- **Half-Full and Almost Full/Almost Empty Flags**
- **Support Clock Frequencies Up To 15 MHz**
- **Characterized for Operation Over the Industrial Temperature Range (–40°C to 85°C)**
- **Access Times of 20 ns**
- **Low-Power Advanced CMOS Technology**
- **Available in 24-Pin SOIC (DW) Package**

**DW PACKAGE**
**(TOP VIEW)**




PRODUCT PREVIEW

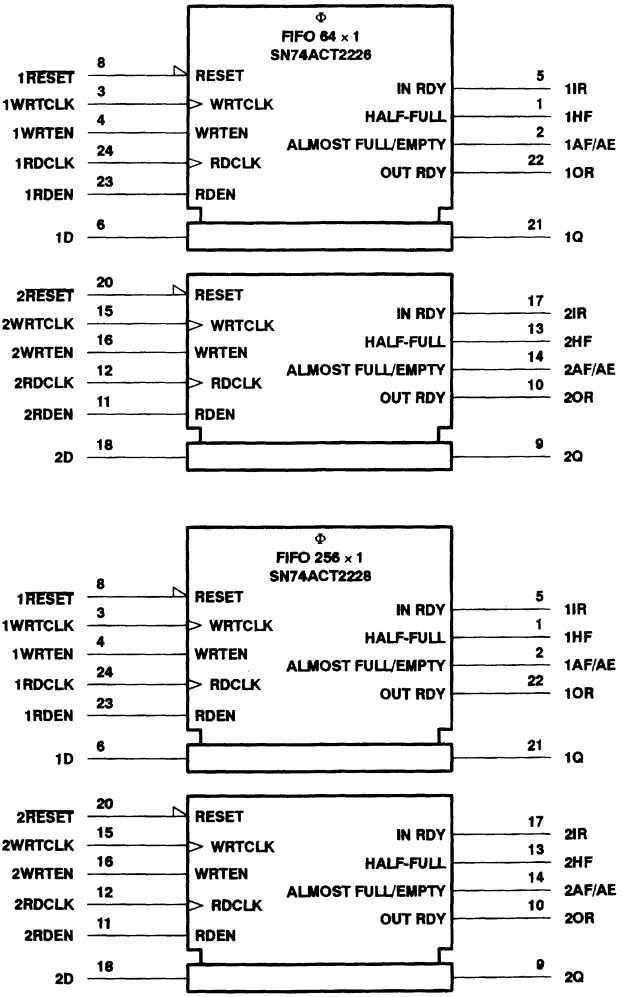
## description

The SN74ACT2226 and SN74ACT2228 are dual FIFOs suited for a wide range of serial data buffering applications including elastic stores for frequencies up to T2 telecommunication rates. Each FIFO on the chip is arranged as 64 × 1 (SN74ACT2226) or 256 × 1 (SN74ACT2228) and has control signals and status flags for independent operation. Output flags per FIFO include input ready (1IR or 2IR), output ready (1OR or 2OR), half-full (1HF or 2HF), and almost full/almost empty (1AF/AE or 2AF/AE).

Serial data is written into a FIFO on the low-to-high transition of the write-clock (1WRTCLK or 2WRTCLK) input when the write enable (1WRTEN or 2WRTEN) input and input ready flag (1IR or 2IR) output are both high. Serial data is read from a FIFO on the low-to-high transition of the read clock (1RDCLK or 2RDCLK) input when the read enable (1RDEN or 2RDEN) input and output ready flag (1OR or 2OR) output are both high. The read and write clocks of a FIFO may be asynchronous to one another.

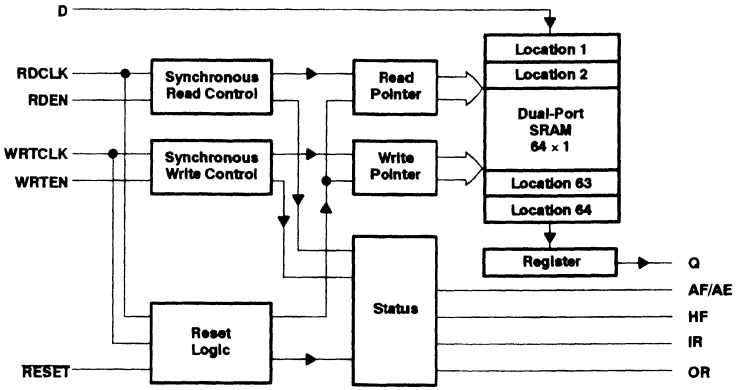
PRODUCT PREVIEW

## logic symbols†

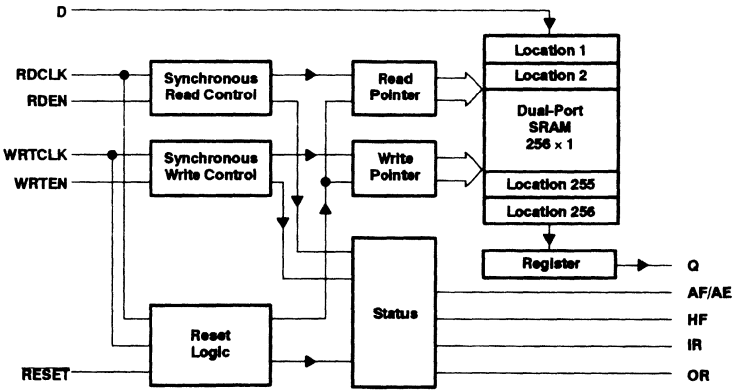



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN74ACT2226 functional block diagram (each FIFO)**




**SN74ACT2228 functional block diagram (each FIFO)**




PRODUCT PREVIEW

## Terminal Functions

| PIN NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| 1AF/AE<br>2AF/AE | 2<br>14 | O | Almost full/almost empty flag. AF/AE is high when the memory is eight locations or less from a full or empty state. AF/AE is set high after reset. |
| 1D, 2D | 6, 18 | I | Data input |
| GND | 7 | | Ground |
| 1HF<br>2HF | 1<br>15 | O | Half-full flag. HF is high when the number of bits stored in memory is greater than or equal to half the FIFO depth. HF is set low after reset. |
| 1IR<br>2IR | 5<br>17 | O | Input ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is set low during reset and is set high on the second low-to-high transition of WRTCLK after reset. |
| 1OR<br>2OR | 22<br>10 | O | Output ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on the data output when OR is high. OR is set low during reset and set high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory. |
| 1Q<br>2Q | 21<br>9 | O | Data outputs. After the first valid write to empty memory, the first bit is output on the third rising edge of RDCLK. OR for the FIFO is also asserted high at this time to indicate ready data. |
| 1RDCLK<br>2RDCLK | 24<br>12 | I | Read clock. RDCLK is a continuous clock and may be independent of any other clock on the device. A low-to-high transition of RDCLK reads data from memory when the FIFO's RDEN and OR are high. OR is synchronous with the low-to-high transition of RDCLK. |
| 1RDEN<br>2RDEN | 23<br>11 | I | Read enable. When the RDEN and OR of a FIFO are high, data is read from the FIFO on the low-to-high transition of RDCLK. |
| 1RESET<br>2RESET | 8<br>20 | I | Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high. |
| $V_{CC}$ | 19 | | Supply voltage |
| 1WRTCLK<br>2WRTCLK | 3<br>15 | I | Write clock. WRTCLK is a continuous clock and may be independent of any other clock on the device. A low-to-high transition of WRTCLK writes data to memory when WRTEN and IR are high. IR is synchronous with the low-to-high transition of WRTCLK. |
| 1WRTEN<br>2WRTEN | 4<br>16 | I | Write enable. When WRTEN and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. |

## timing diagrams

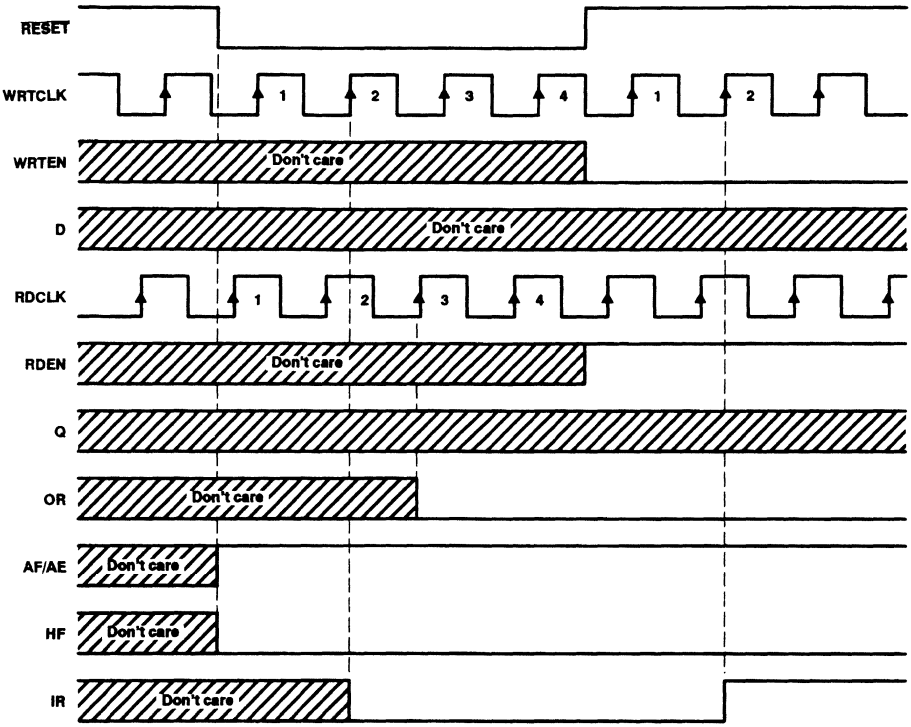
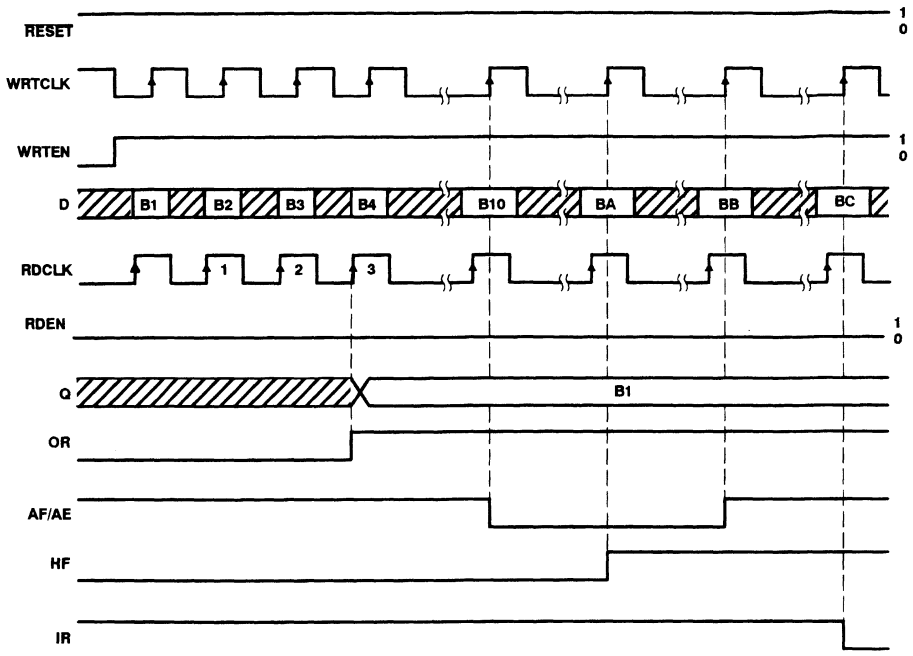


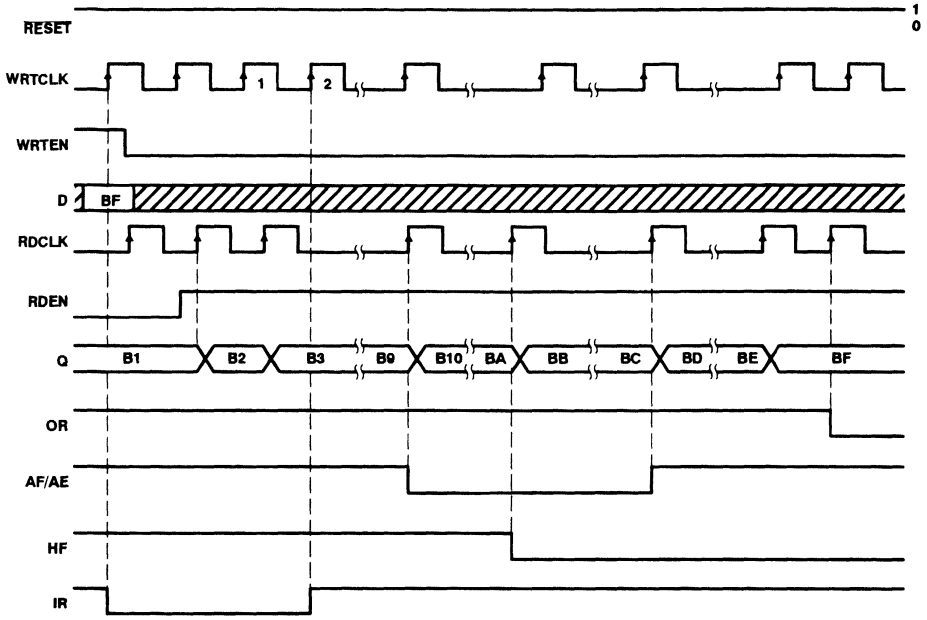

**Figure 1. FIFO Reset**




DATA BIT NUMBER BASED ON FIFO DEPTH

| DEVICE | DATA BIT | | |
|---|---|---|---|
| | BA | BB | BC |
| SN74ACT2226 | B33 | B57 | B65 |
| SN74ACT2228 | B129 | B249 | B257 |

**Figure 2. FIFO Write**




**DATA BIT NUMBER BASED ON FIFO DEPTH**

| DEVICE | DATA BIT | | | | | |
|---|---|---|---|---|---|---|
| | BA | BB | BC | BD | BE | BF |
| SN74ACT2226 | B33 | B34 | B56 | B57 | B64 | B65 |
| SN74ACT2228 | B129 | B130 | B248 | B249 | B256 | B257 |

**Figure 3. FIFO Read**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Operating free-air temperature range ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

### recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | mA |
| | | Flags | | 8 | |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$‡ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

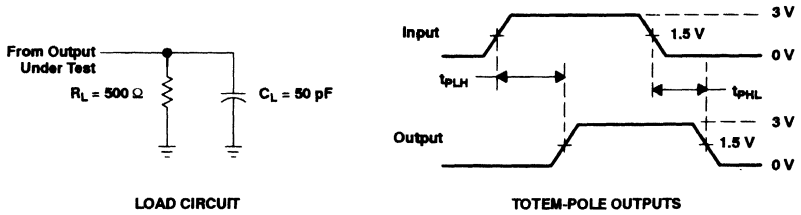
### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{max}$ | 1WRTCLK, 2WRTCLK, or 1RDCLK, 2RDCLK | | 15 | | | MHz |
| $t_{pd}$ | 1RDCLK↑, 2RDCLK↑ | 1Q, 2Q | | | 20 | ns |
| $t_{pd}$ | 1WRTCLK↑, 2WRTCLK↑ | 1IR, 2IR | | | 20 | ns |
| $t_{pd}$ | 1RDCLK↑, 2RDCLK↑ | 1OR, 2OR | | | 20 | ns |
| $t_{pd}$ | 1WRTCLK↑, 2WRTCLK↑ | 1AF/AE, 2AF/AE | | | 20 | ns |
| $t_{pd}$ | 1RDCLK↑, 2RDCLK↑ | 1AF/AE, 2AF/AE | | | 20 | ns |
| $t_{PLH}$ | 1WRTCLK↑, 2WRTCLK↑ | 1HF, 2HF | | | 20 | ns |
| $t_{PHL}$ | 1RDCLK↑, 2RDCLK↑ | | | | 20 | |
| $t_{PLH}$ | 1$\overline{RESET}$, 2$\overline{RESET}$ low | 1AF/AE, 2AF/AE | | | | ns |
| $t_{PHL}$ | | 1HF, 2HF | | | | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, | f = 5 MHz | | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT

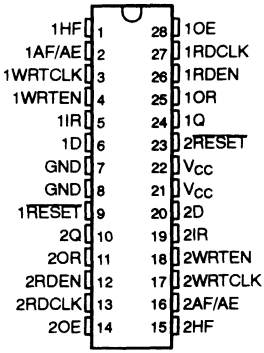
TOTEM-POLE OUTPUTS

**Figure 4. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Dual Independent FIFOs Organized As:**
  - **64 Words by 1 Bit Each – SN74ACT2227**
  - **256 Words by 1 Bit Each – SN74ACT2229**
- **Free-Running Read and Write Clocks May Be Asynchronous or Coincident on Each FIFO**
- **Input Ready Flags Synchronized to Write Clocks**
- **Output Ready Flags Synchronized to Read Clocks**
- **Half-Full and Almost Full/Almost Empty Flags**
- **Characterized for Operation Over the Industrial Temperature Range (–40°C to 85°C)**
- **Support Clock Frequencies Up To 60 MHz**
- **Access Times of 12 ns**
- **3-State Data Outputs**
- **Low-Power Advanced CMOS Technology**
- **Available in 28-Pin SOIC (DW) or SSOP (DL) Packages**

**DW OR DL PACKAGE**
**(TOP VIEW)**



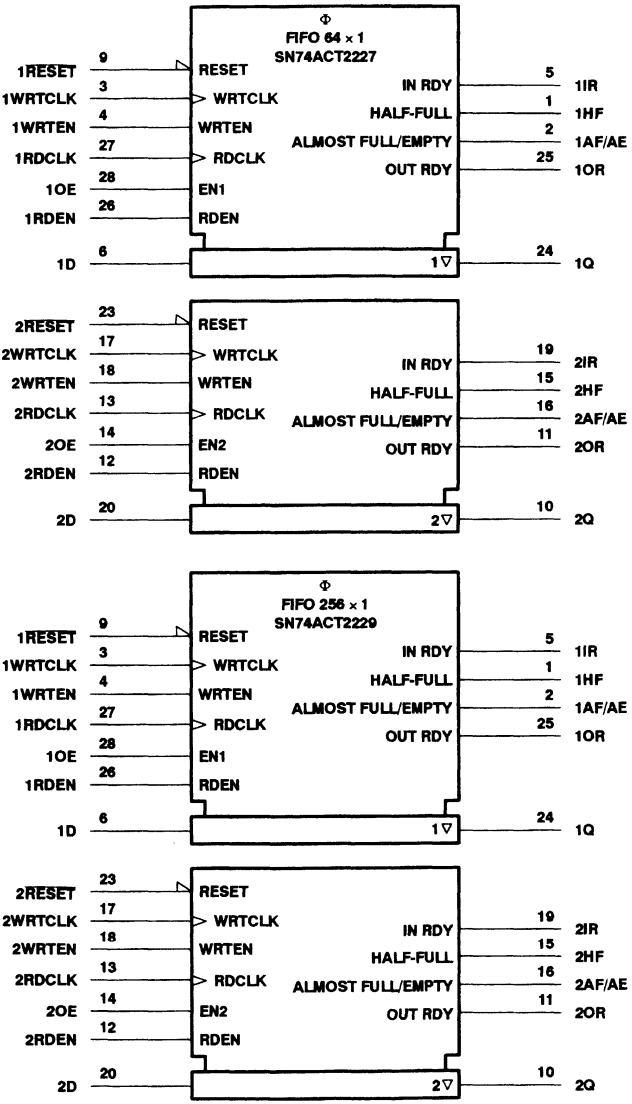

## description

The SN74ACT2227 and SN74ACT2229 are dual FIFOs suited for a wide range of serial data buffering applications including elastic stores for frequencies up to OC-1 telecommunication rates. Each FIFO on the chip is arranged as 64 × 1 (SN74ACT2227) or 256 × 1 (SN74ACT2229) and has control signals and status flags for independent operation. Output flags per FIFO include input ready (1IR or 2IR), output ready (1OR or 2OR), half-full (1HF or 2HF), and almost full/almost empty (1AF/AE or 2AF/AE).

Serial data is written into a FIFO on the low-to-high transition of the write-clock (1WRTCLK or 2WRTCLK) input when the write enable (1WRTEN or 2WRTEN) input and input ready flag (1IR or 2IR) output are both high. Serial data is read from a FIFO on the low-to-high transition of the read clock (1RDCLK or 2RDCLK) input when the read enable (1RDEN or 2RDEN) input and output ready flag (1OR or 2OR) output are both high. The read and write clocks of a FIFO may be asynchronous to one another. A FIFO data output (1Q or 2Q) is in the high-impedance state when its output-enable (1OE or 2OE) input is low.

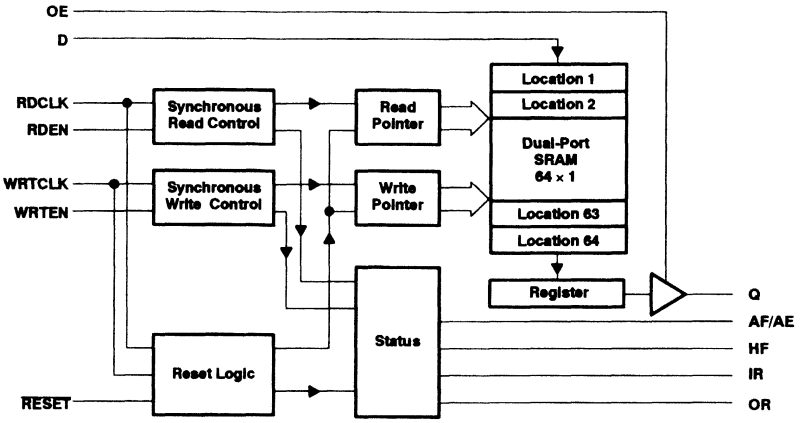
PRODUCT PREVIEW

## logic symbols†

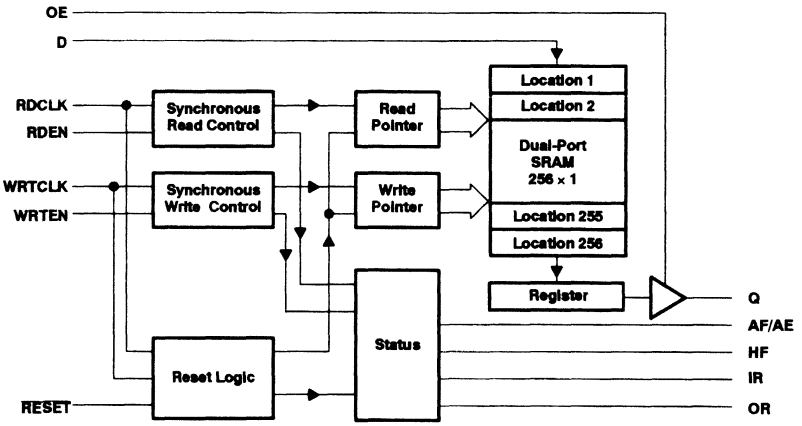



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### SN74ACT2227 functional block diagram (each FIFO)




### SN74ACT2229 functional block diagram (each FIFO)




PRODUCT PREVIEW

## Terminal Functions

| PIN NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| 1AF/AE<br>2AF/AE | 2<br>16 | O | Almost full/almost empty flag. AF/AE is high when the memory is eight locations or less from a full or empty state. AF/AE is set high after reset. |
| 1D, 2D | 6, 20 | I | Data input |
| GND | 7, 8 | | Ground |
| 1HF<br>2HF | 1<br>15 | O | Half-full flag. HF is high when the number of bits stored in memory is greater than or equal to half the FIFO depth. HF is set low after reset. |
| 1IR<br>2IR | 5<br>19 | O | Input ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is set low during reset and is set high on the second low-to-high transition of WRTCLK after reset. |
| 1OE<br>2OE | 28<br>14 | I | Output enable. The data output of a FIFO is active when OE is high and in the high-impedance state when OE is low. |
| 1OR<br>2OR | 25<br>11 | O | Output ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on the data output when OR is high. OR is set low during reset and set high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory. |
| 1Q<br>2Q | 24<br>10 | O | Data outputs. After the first valid write to empty memory, the first bit is output on the third rising edge of RDCLK. OR for the FIFO is also asserted high at this time to indicate ready data. |
| 1RDCLK<br>2RDCLK | 27<br>13 | I | Read clock. RDCLK is a continuous clock and may be independent of any other clock on the device. A low-to-high transition of RDCLK reads data from memory when the FIFO's RDEN and OR are high. OR is synchronous with the low-to-high transition of RDCLK. |
| 1RDEN<br>2RDEN | 26<br>12 | I | Read enable. When the RDEN and OR of a FIFO are high, data is read from the FIFO on the low-to-high transition of RDCLK. |
| 1$\overline{\text{RESET}}$<br>2$\overline{\text{RESET}}$ | 9<br>23 | I | Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high. |
| $V_{CC}$ | 21,<br>22 | | Supply voltage |
| 1WRTCLK<br>2WRTCLK | 3<br>17 | I | Write clock. WRTCLK is a continuous clock and may be independent of any other clock on the device. A low-to-high transition of WRTCLK writes data to memory when WRTEN and IR are high. IR is synchronous with the low-to-high transition of WRTCLK. |
| 1WRTEN<br>2WRTEN | 4<br>18 | I | Write enable. When WRTEN and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. |

PRODUCT PREVIEW

**timing diagrams**

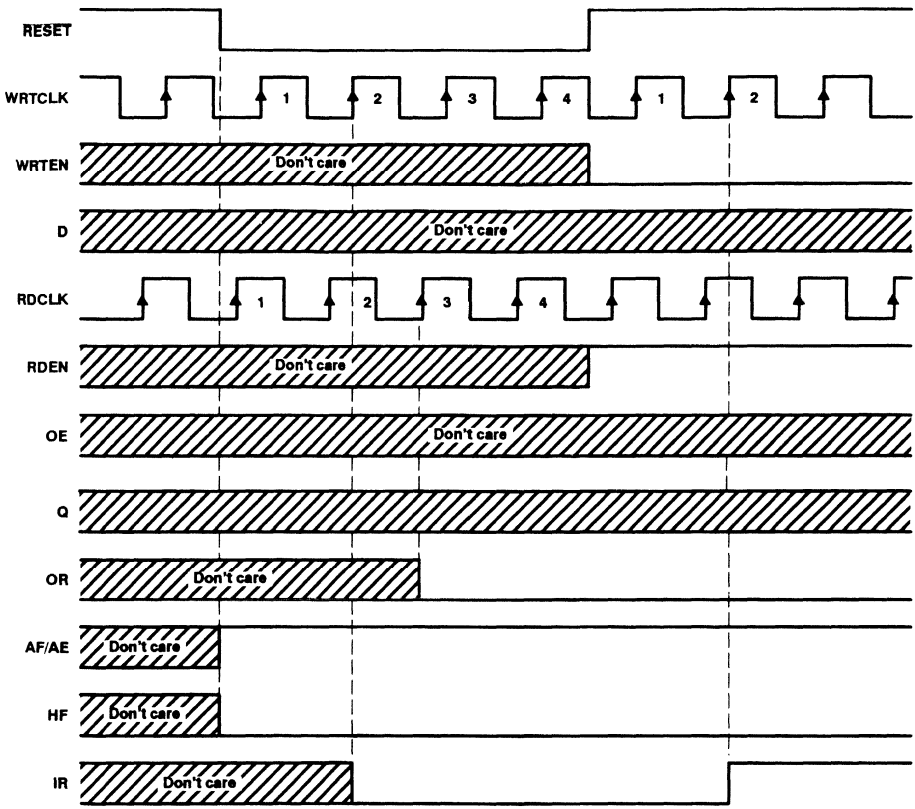
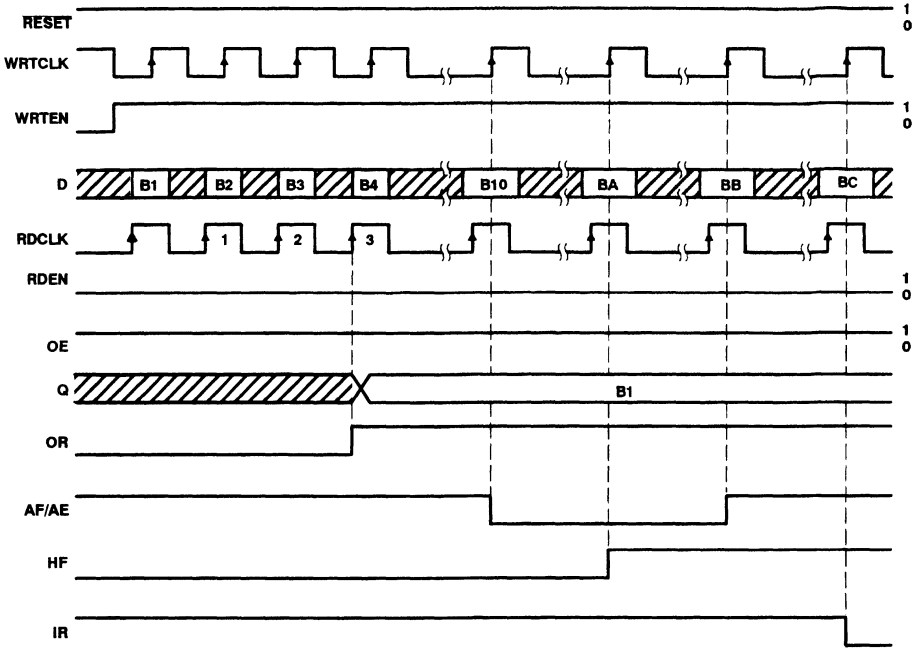


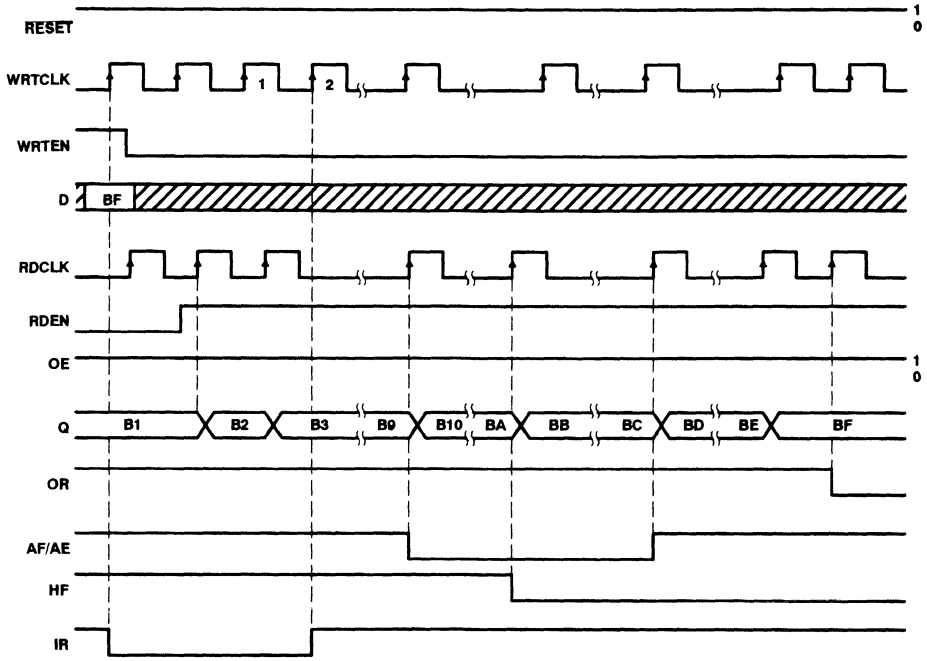

Figure 1. FIFO Reset




DATA BIT NUMBER BASED ON FIFO DEPTH

| DEVICE | DATA BIT | | |
|---|---|---|---|
| | BA | BB | BC |
| SN74ACT2227 | B33 | B57 | B65 |
| SN74ACT2229 | B129 | B249 | B257 |

**Figure 2. FIFO Write**




DATA BIT NUMBER BASED ON FIFO DEPTH

| DEVICE | DATA BIT | | | | | |
|---|---|---|---|---|---|---|
| | BA | BB | BC | BD | BE | BF |
| SN74ACT2227 | B33 | B34 | B56 | B57 | B64 | B65 |
| SN74ACT2229 | B129 | B130 | B248 | B249 | B256 | B257 |

**Figure 3. FIFO Read**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs, flags | | −8 | mA |
| $I_{OL}$ | Low-level output current | Q outputs | | 16 | mA |
| | | Flags | | 8 | |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −8 mA | 2.4 | | | V |
| $V_{OL}$ | Flags | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| | Q outputs | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

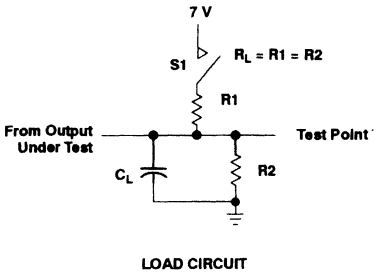
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{max}$ | 1WRTCLK, 2WRTCLK, or 1RDCLK, 2RDCLK | | 60 | | | MHz |
| $t_{pd}$ | 1RDCLK↑, 2RDCLK↑ | 1Q, 2Q | | | 12 | ns |
| $t_{pd}$ | 1WRTCLK↑, 2WRTCLK↑ | 1IR, 2IR | | | 10 | ns |
| $t_{pd}$ | 1RDCLK↑, 2RDCLK↑ | 1OR, 2OR | | | 10 | ns |
| $t_{pd}$ | 1WRTCLK↑, 2WRTCLK↑ | 1AF/AE, 2AF/AE | | | 17 | ns |
| $t_{pd}$ | 1RDCLK↑, 2RDCLK↑ | 1AF/AE, 2AF/AE | | | 18 | ns |
| $t_{PLH}$ | 1WRTCLK↑, 2WRTCLK↑ | 1HF, 2HF | | | 15 | ns |
| $t_{PHL}$ | 1RDCLK↑, 2RDCLK↑ | | | | 19 | |
| $t_{PLH}$ | 1$\overline{RESET}$, 2$\overline{RESET}$ low | 1AF/AE, 2AF/AE | | | | ns |
| $t_{PHL}$ | | 1HF, 2HF | | | | |
| $t_{en}$ | 1OE, 2OE | 1Q, 2Q | | | 14 | ns |
| $t_{dis}$ | | | | | 14 | |

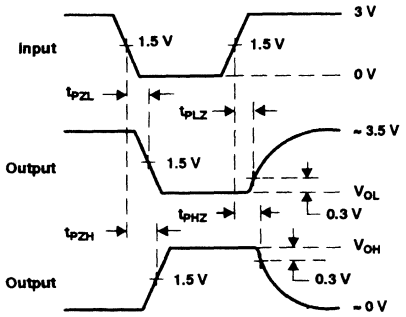
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 5 MHz | | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

| PARAMETER | | R1, R2 | $C_L$† | S1 |
|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 500 Ω | 50 pF | Open |
| | $t_{PZL}$ | | | Closed |
| $t_{dis}$ | $t_{PHZ}$ | 500 Ω | 50 pF | Open |
| | $t_{PLZ}$ | | | Closed |
| $t_{pd}$ | | 500 Ω | 50 pF | Open |

† Includes probe and test fixture capacitance.

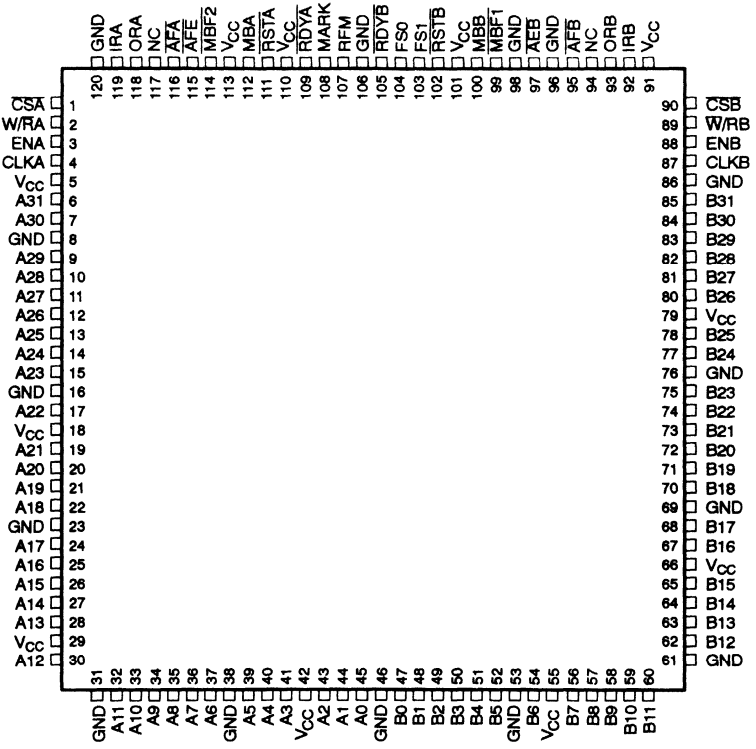
**Figure 4. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

JUNE 1992

- Free-Running CLKA and CLKB May Be Asynchronous or Coincident
- Two Independent 512 × 32 Clocked FIFOs Buffering Data in Opposite Directions
- Read Retransmit Capability From FIFO on Port B
- Mailbox Bypass Register for Each FIFO
- Programmable Almost Full and Almost Empty Flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{AEA}$, and $\overline{AFA}$ Flags Synchronized by CLKA
- IRB, ORB, $\overline{AEB}$, and $\overline{AFB}$ Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 12 ns
- Available in 132-Pin Quad Flatpack (PQ) or Space-Saving 120-Pin Shrink Quad Flatpack (PCB)

**PCB PACKAGE**
**(TOP VIEW)**




NC – No internal connection

PRODUCT PREVIEW

JUNE 1992

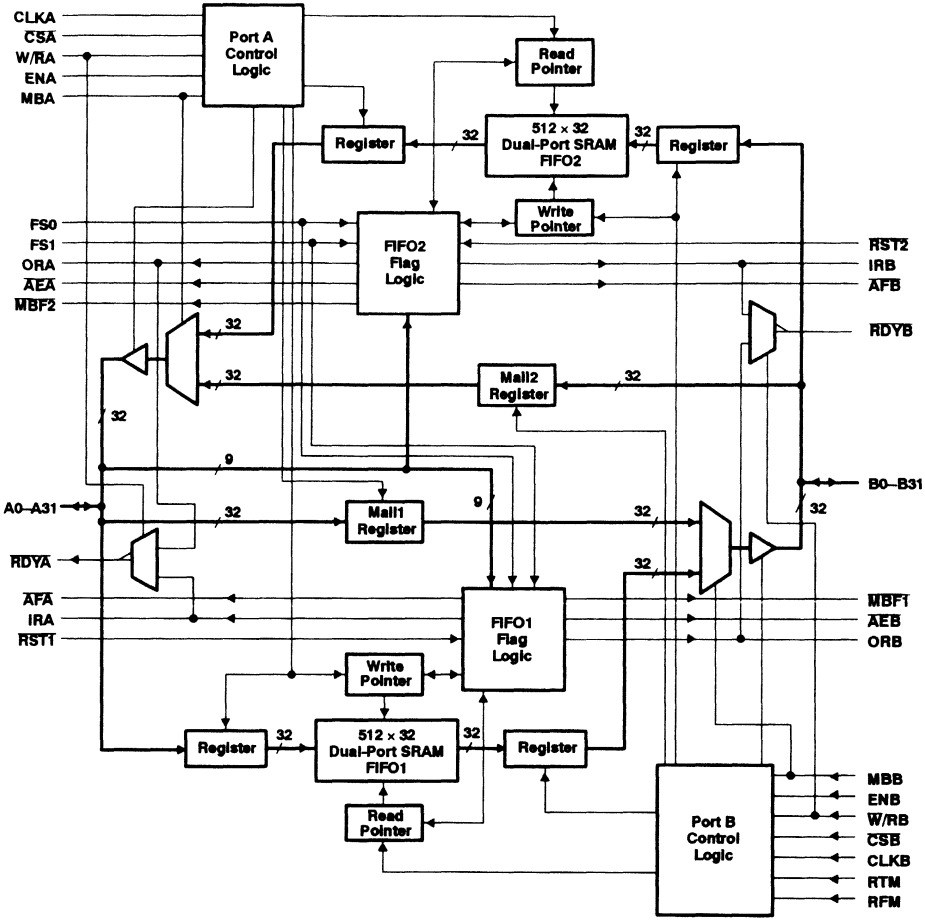
## description

The SN74ACT7821 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12 ns. Two independent 512 x 32 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. The FIFO memory buffering data from port A to port B has retransmit capability, which allows previously read data to be accessed again. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port may bypass the FIFOs via two 32-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices may be used in parallel to create wider data paths.

The SN74ACT7821 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input ready flag and almost full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output ready flag and almost empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offsets for the almost full and almost empty flags of both FIFOs can be programmed from port A.

## functional block diagram




PRODUCT PREVIEW

JUNE 1992

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A31 | I/O | Port A data. 32-bit bidirectional data port for side A. |
| $\overline{AEA}$ | O | FIFO2 almost empty flag. Programmable flag synchronized to CLKA. It is low when the number of words in FIFO2 is less than or equal to the selected value. |
| $\overline{AEB}$ | O | FIFO1 almost empty flag. Programmable flag synchronized to CLKB. It is low when the number of words in FIFO1 is less than or equal to the selected value. |
| $\overline{AFA}$ | O | FIFO1 almost full flag. Programmable flag synchronized to CLKA. It is low when the number of empty locations in FIFO1 is less than or equal to the selected value. |
| $\overline{AFB}$ | O | FIFO2 almost full flag. Programmable flag synchronized to CLKB. It is low when the number of empty locations in FIFO2 is less than or equal to the selected value. |
| B0–B31 | I/O | Port B data. 32-bit bidirectional data port for side B. |
| CLKA | I | Port A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and may be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$ are synchronous to the low-to-high transition of CLKA. |
| CLKB | I | Port B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and may be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronous to the low-to-high transition of CLKB. |
| $\overline{CSA}$ | I | Port A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A31 outputs are in the high-impedance state when $\overline{CSA}$ is high. |
| $\overline{CSB}$ | I | Port B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B31 outputs are in the high-impedance state when $\overline{CSB}$ is high. |
| ENA | I | Port A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A. |
| ENB | I | Port B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B. |
| FS1, FS0 | I | Flag offset selects. The low-to-high transition of a FIFO's reset input latches the value of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO's almost full and almost empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{RST1}$ and $\overline{RST2}$ go high, the first four writes to FIFO1 program the almost full and almost empty offsets for both FIFOs. |
| IRA | O | FIFO1 input ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. When FIFO1 is in retransmit mode, IRA indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset. |
| IRB | O | FIFO2 input ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full, and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset. |
| MBA | I | Port A mailbox select. A high level chooses a mailbox register for a port A read or write operation. When the A0–A31 outputs are active, a high level on MBA selects data from the mail2 register for output, and a low level selects FIFO2 data for output. |
| MBB | I | Port B mailbox select. A high level chooses a mailbox register for a port B read or write operation. When the B0–B31 outputs are active, a high level on MBB selects data from the mail1 register for output, and a low level selects FIFO1 data for output. |
| $\overline{MBF1}$ | O | Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port B read is selected and MBB is high. $\overline{MBF1}$ is set high when FIFO1 is reset. |
| $\overline{MBF2}$ | O | Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port A read is selected and MBA is high. $\overline{MBF2}$ is set high when FIFO2 is reset. |
| ORA | O | FIFO2 output ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty, and reads are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory. |

**Terminal Functions (continued)**

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| ORB | O | FIFO1 output ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty, and reads are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory. |
| RDYA | O | Port A ready. A high on W/$\overline{RA}$ selects the inverted state of IRA for output on $\overline{RDYA}$, and a low on W/$\overline{RA}$ selects the inverted state of ORA for output on $\overline{RDYA}$. |
| RDYB | O | Port B ready. A low on $\overline{W}$/RB selects the inverted state of IRB for output on $\overline{RDYB}$, and a high on $\overline{W}$/RB selects the inverted state of ORB for output on $\overline{RDYB}$. |
| RFM | I | FIFO1 read from mark. When FIFO1 is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the FIFO1 read pointer to the retransmit location and output the first retransmit data. |
| $\overline{RST1}$ | I | FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST1}$ is low. The low-to-high transition of $\overline{RST1}$ latches the status of FS0 and FS1 for $\overline{AFA}$ and $\overline{AEB}$ offset selection. |
| $\overline{RST2}$ | I | FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST2}$ is low. The low-to-high transition of $\overline{RST2}$ latches the status of FS0 and FS1 for $\overline{AFB}$ and $\overline{AEA}$ offset selection. |
| RTM | I | FIFO1 retransmit mode. When RTM is high and valid data is present on the output of FIFO1, a low-to-high transition of CLKB selects the data for the beginning of a FIFO1 retransmit. The selected position remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, which takes FIFO out of retransmit mode. |
| W/$\overline{RA}$ | I | Port A write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A31 outputs are in the high-impedance state when W/$\overline{RA}$ is high. |
| $\overline{W}$/RB | I | Port B $\overline{write}$/read select. A low selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B31 outputs are in the high-impedance state when $\overline{W}$/RB is low. |

## FIFO function

The state of the A0–A31 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to FIFO1 from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, MBA is low, ENA is high, and the IRA flag is high. Data is read from FIFO2 to the A0–A31 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, MBA is low, ENA is high, and the ORA flag is high.

The state of the B0–B31 outputs is controlled by $\overline{CSB}$ and $\overline{W}$/RB. When $\overline{CSB}$ is low and $\overline{W}$/RB is high, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. Data is written to FIFO2 from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, MBB is low, ENB is high, and the IRB flag is high. Data is read from FIFO1 to the B0–B31 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is high, MBB is low, ENB is high, and the ORB flag is high.

The setup and hold time constraints to the port clocks for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, $\overline{W}$/RB) are for enabling write and read operations and are not related to high-impedance control of the data outputs. If the master enable signal for a port (ENA or ENB) is set low during a clock cycle, the chip select and write/read select may switch at any time during the cycle to change the state of the data outputs.

Each FIFO flag is two-stage synchronized to a port clock for use as a reliable synchronous control signal. CLKA synchronizes the status of the output ready flag (ORA) and almost empty flag ($\overline{AEA}$) of FIFO2 and the input ready flag (IRA) and almost full flag ($\overline{AFA}$) of FIFO1. CLKB synchronizes the status of the output ready flag (ORB) and almost empty flag ($\overline{AEB}$) of FIFO1 and the input ready flag (IRB) and almost full flag ($\overline{AFB}$) of FIFO2.

### FIFO function (continued)

When the input ready flag (IRA, IRB) of a port is low, the FIFO receiving input from the port is full, and writes are disabled to its array. When the output ready flag (ORA, ORB) of a port is low, the FIFO that outputs data to the port is empty, and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO's output register when the port's output ready flag is asserted (high). When the memory is read empty and the output ready flag is forced low, the last valid data remains on the FIFO outputs until the output ready flag is asserted (high) again. In this way, a high on the output ready flag indicates that new data is present on the FIFO outputs. The ready flag ($\overline{RDYA}$ or $\overline{RDYB}$) of a port is low when the FIFO selected by the write/read select is ready for data transfer.

### mailbox registers

A 32-bit word may be exchanged between ports and circumvent the normal FIFO path. The mailbox select inputs (MBA, MBB) choose between a mail register and a FIFO for a port data transfer operation. A0–A31 data is written to the mail1 register on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is high, ENA is high, and MBA is high. B0–B31 data is written to the mail2 register on a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, ENB is high, and MBB is high.

When data is written to a mail register, its mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) is set low. The $\overline{MBF1}$ flag is set back high on a low-to-high transition of CLKB when a read is selected for port B and the MBB input is high. The $\overline{MBF2}$ flag is set high on a low-to-high transition of CLKA when a read is selected for port A and the MBA input is high. The data in a mailbox register remains intact after it is read and changes only when new data is written to the register. When a port's data output registers are active, a high on the mailbox enable (MBA or MBB) selects mail data to be output on the port, and a low selects FIFO data for output.

### reset

The FIFO memories on the SN74ACT7821 are reset separately by taking their reset input ($\overline{RST1}$ or $\overline{RST2}$) low for at least four CLKA and four CLKB low-to-high transitions. The reset inputs may be asynchronous with respect to either clock. This resets the internal read and write pointers to the initial location and forces the FIFO's $\overline{AF}$ flag high and IR, OR, and $\overline{AE}$ flags low. Resetting a FIFO also forces the flag of its parallel mailbox register high. Data outputs of the FIFO and mailbox register are not reset to any specific logic level. Both FIFOs must be reset upon power up.

### almost full and almost empty flags

Three default values are available for the offsets of the almost full and almost empty flags of a FIFO, or values can be programmed for each flag from port A. The flag select inputs (FS0, FS1) are sampled for each FIFO by the low-to-high transition of its reset input. If the values of FS0 and FS1 select a preset value at the time of the rising edge of $\overline{RST1}$ or $\overline{RST2}$, the value is set as the offset for the almost full and almost empty flags of the FIFO.

To program the almost full and almost empty flags of FIFO1 and FIFO2, both FIFOs should be reset simultaneously with the flag select inputs low during the low-to-high transition of the reset signals. After this reset cycle, IRA is forced high on the second low-to-high transition of CLKA, but IRB remains low until the programming is complete. The first four writes from port A to FIFO1 program offsets for flags in the order of $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$ and $\overline{AFB}$. The offsets may be programmed from 1 to 508. The IRB flag is asserted high by the second CLKB low-to-high transition after the $\overline{AFB}$ offset is programmed. The fifth write from port A to FIFO1 stores the first word in its memory.

An almost empty flag is low when the number of 32-bit words stored in its FIFO is less than or equal to the flag's offset value. An almost full flag is low when the number of empty locations left in its FIFO is less than or equal to the flag's offset value. Data in the output register of a FIFO has been read from memory, and its previous location is free.

PRODUCT PREVIEW

FLAG PROGRAMMING TABLE

| FS1 | FS0 | RST1 | RST2 | FIFO1 OFFSET | FIFO2 OFFSET |
|---|---|---|---|---|---|
| H | H | ↑ | X | 64 | X |
| H | H | X | ↑ | X | 64 |
| H | L | ↑ | X | 16 | X |
| H | L | X | ↑ | X | 16 |
| L | H | ↑ | X | 8 | X |
| L | H | X | ↑ | X | 8 |
| L | L | ↑ | ↑ | Programmed from port A | Programmed from port A |

## retransmit

A selected portion of the data in FIFO1 may be read repeatedly when FIFO1 is in retransmit mode. The FIFO is put in retransmit mode by asserting the retransmit mode input (RTM) high during a low-to-high transition of CLKB. If valid data is present on the bus at this time, it is the first data to be output when retransmit is activated. FIFO1 is in retransmit mode until RTM is low during a low-to-high transition of CLKB. While the FIFO is in retransmit mode, the FIFO is filled by the 512th word written after the first retransmit data.

When FIFO1 is in retransmit mode, a high on the read from mark input (RFM) enables a low-to-high transition of CLKB to begin retransmit. This clock edge resets the read pointer to the first retransmit location and outputs the first retransmit data. Data may be retransmitted from the selected starting position repeatedly. A new retransmit starting position may be selected after taking FIFO1 out of retransmit mode by asserting RTM high during a low-to-high transition of CLKB when the selected starting data is present of the FIFO1 outputs.

## recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −4 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = − 4 mA | 2.4 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{OZ}$ | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | ±5 | μA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | 400 | μA |
| $\Delta I_{CC}$‡ | $V_{CC}$ = 5.5 V, | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | $V_I$ = 0, | f = 1 MHz | | 4 | | pF |
| $C_o$ | $V_O$ = 0, | f = 1 MHz | | 8 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

PRODUCT PREVIEW

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 30 pF (unless otherwise noted)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7821-15 | | 'ACT7821-20 | | 'ACT7821-25 | | 'ACT7821-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKA or CLKB | | 67 | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | CLKA↑ | A0–A31 | | 12 | | 13 | | 15 | | 17 | ns |
| | CLKB↑ | B0–B31 | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | IRA | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | IRB | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | ORA | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | ORB | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | $\overline{AFA}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | $\overline{AFB}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | $\overline{AEA}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | $\overline{AEB}$ | | 12 | | 13 | | 15 | | 17 | |
| $t_{PHL}$ | CLKA↑ | $\overline{MBF1}$ | | 11 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKB↑ | | | 11 | | 12 | | 14 | | 16 | |
| $t_{PHL}$ | CLKB↑ | $\overline{MBF2}$ | | 11 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKA↑ | | | 11 | | 12 | | 14 | | 16 | |
| $t_{pd}$ | MBA | A0–A31 | | 11 | | 12 | | 14 | | 16 | ns |
| | $\overline{MBB}$ | B0–B31 | | 11 | | 12 | | 14 | | 16 | |
| $t_{PHL}$ | $\overline{RST1}$ | $\overline{AEB}$ | | | | | | | | | ns |
| | $\overline{RST2}$ | $\overline{AEA}$ | | | | | | | | | |
| $t_{PLH}$ | $\overline{RST1}$ | $\overline{AFA}$ | | | | | | | | | ns |
| | $\overline{RST2}$ | $\overline{AFB}$ | | | | | | | | | |
| $t_{PLH}$ | $\overline{RST1}$ | $\overline{MBF1}$ | | | | | | | | | ns |
| | $\overline{RST2}$ | $\overline{MBF2}$ | | | | | | | | | |
| $t_{en}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A31 | | | | | | | | | ns |
| | $\overline{CSB}$, $\overline{W}$/RB | B0–B31 | | | | | | | | | |
| $t_{dis}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A31 | | | | | | | | | ns |
| | $\overline{CSB}$, $\overline{W}$/RB | B0–B31 | | | | | | | | | |

PRODUCT PREVIEW

JUNE 1992

- **Free-Running CLKA and CLKB May Be Asynchronous or Coincident**
- **Two Independent 512 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Programmable Almost Full and Almost Empty Flags**
- **Microprocessor Interface Control Logic**
- **IRA, ORA, $\overline{AEA}$, and $\overline{AFA}$ Flags Synchronized by CLKA**
- **IRB, ORB, $\overline{AEB}$, and $\overline{AFB}$ Flags Synchronized by CLKB**
- **Low-Power 0.8-Micron Advanced CMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 12 ns**
- **Available in 132-Pin Quad Flatpack (PQ) or Space-Saving 120-Pin Shrink Quad Flatpack (PCB)**

## description

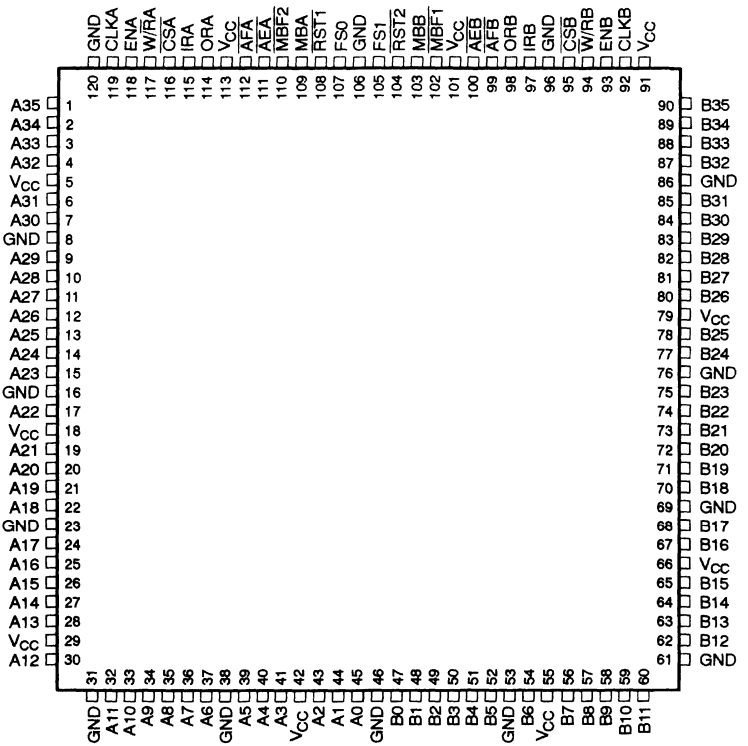
The SN74ACT7822 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12 ns. Two independent 512 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port may bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices may be used in parallel to create wider data paths.

The SN74ACT7822 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input ready flag and almost full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output ready flag and almost empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offsets for the almost full and almost empty flags of both FIFOs can be programmed from port A.

PRODUCT PREVIEW

PCB PACKAGE
(TOP VIEW)

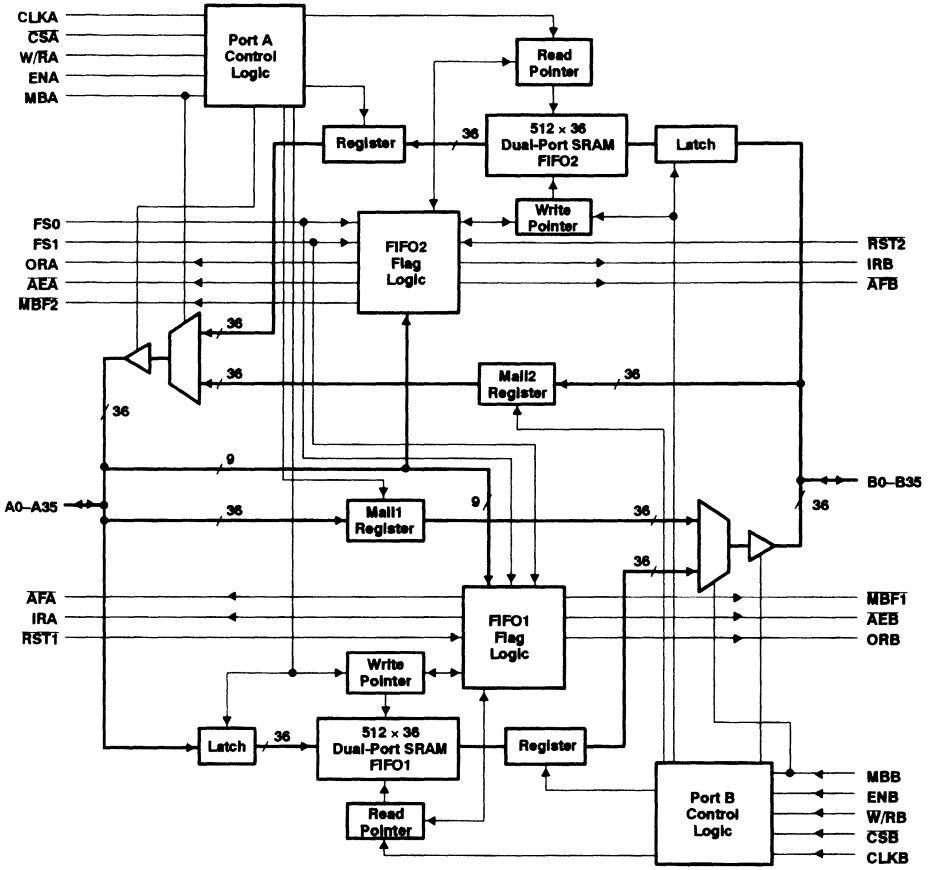



PRODUCT PREVIEW



TEXAS INSTRUMENTS

## functional block diagram



## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A35 | I/O | Port A data. 36-bit bidirectional data port for side A. |
| $\overline{AEA}$ | O | FIFO2 almost empty flag. Programmable flag synchronized to CLKA. It is low when the number of words in FIFO2 is less than or equal to the selected value. |
| $\overline{AEB}$ | O | FIFO1 almost empty flag. Programmable flag synchronized to CLKB. It is low when the number of words in FIFO1 is less than or equal to the selected value. |
| $\overline{AFA}$ | O | FIFO1 almost full flag. Programmable flag synchronized to CLKA. It is low when the number of empty locations in FIFO1 is less than or equal to the selected value. |
| $\overline{AFB}$ | O | FIFO2 almost full flag. Programmable flag synchronized to CLKB. It is low when the number of empty locations in FIFO2 is less than or equal to the selected value. |
| B0–B35 | I/O | Port B data. 36-bit bidirectional data port for side B. |
| CLKA | I | Port A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and may be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronous to the low-to-high transition of CLKA. |
| CLKB | I | Port B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and may be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronous to the low-to-high transition of CLKB. |
| $\overline{CSA}$ | I | Port A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high. |
| $\overline{CSB}$ | I | Port B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high. |
| ENA | I | Port A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A. |
| ENB | I | Port B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B. |
| FS1, FS0 | I | Flag offset selects. The low-to-high transition of a FIFO's reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO's almost full and almost empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{RST1}$ and $\overline{RST2}$ go high, the first four writes to FIFO1 program the almost full and almost empty offsets for both FIFOs. |
| IRA | O | FIFO1 input ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full, and writes to its array are disabled. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset. |
| IRB | O | FIFO2 input ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full, and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset. |
| MBA | I | Port A mailbox select. A high level chooses a mailbox register for a port A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output, and a low level selects FIFO2 data for output. |
| MBB | I | Port B mailbox select. A high level chooses a mailbox register for a port B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output, and a low level selects FIFO1 data for output. |
| $\overline{MBF1}$ | O | Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port B read is selected and MBB is high. $\overline{MBF1}$ is also set high when FIFO1 is reset. |
| $\overline{MBF2}$ | O | Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port A read is selected and MBA is high. $\overline{MBF2}$ is also set high when FIFO2 is reset. |
| ORA | O | FIFO2 output ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty, and reads are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory. |

PRODUCT PREVIEW

**Terminal Functions (continued)**

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| ORB | O | FIFO1 output ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty, and reads are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory. |
| $\overline{RST1}$ | I | FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST1}$ is low. The low-to-high transition of $\overline{RST1}$ latches the status of FS0 and FS1 for $\overline{AFA}$ and $\overline{AEB}$ offset selection. |
| $\overline{RST2}$ | I | FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST2}$ is low. The low-to-high transition of $\overline{RST2}$ latches the status of FS0 and FS1 for $\overline{AFB}$ and $\overline{AEA}$ offset selection. |
| W/$\overline{RA}$ | I | Port A write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high. |
| W/RB | I | Port B $\overline{write}$/read select. A low selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{W}$/RB is low. |

## FIFO function

The state of the A0–A35 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to FIFO1 from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, MBA is low, ENA is high, and the IRA flag is high. Data is read from FIFO2 to the A0–A35 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, MBA is low, ENA is high, and the ORB flag is high.

The state of the B0–B35 outputs is controlled by $\overline{CSB}$ and $\overline{W}$/RB. When $\overline{CSB}$ is low and $\overline{W}$/RB is high, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. Data is written to FIFO2 from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, MBB is low, ENB is high, and the IRB flag is high. Data is read from FIFO1 to the B0–B35 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is high, MBB is low, ENB is high, and the ORB flag is high.

The setup and hold time constraints to the port clocks for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, $\overline{W}$/RB) are for enabling write and read operations and are not related to high-impedance control of the data outputs. If the master enable signal for a port (ENA or ENB) is set low during a clock cycle, the chip select and write/read select may switch at any time during the cycle to change the state of the data outputs.

Each FIFO flag is two-stage synchronized to a port clock for use as a reliable synchronous control signal. CLKA synchronizes the status of the output ready flag (ORA) and almost empty flag ($\overline{AEA}$) of FIFO2 and the input ready flag (IRA) and almost full flag ($\overline{AFA}$) of FIFO1. CLKB synchronizes the status of the output ready flag (ORB) and almost empty flag ($\overline{AEB}$) of FIFO1 and the input ready flag (IRB) and almost full flag ($\overline{AFB}$) of FIFO2.

When the input ready flag (IRA, IRB) of a port is low, the FIFO receiving input from the port is full, and writes are disabled to its array. When the output ready flag (ORA, ORB) of a port is low, the FIFO that outputs data to the port is empty, and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO's output register when the port's output ready flag is asserted (high). When the memory is read empty and the output ready flag is forced low, the last valid data remains on the FIFO outputs until the output ready flag is asserted (high) again. In this way, a high on the output ready flag indicates that new data is present on the FIFO outputs.

### mailbox registers

A 36-bit word may be exchanged between ports and circumvent the normal FIFO path. The mailbox select inputs (MBA, MBB) choose between a mail register and a FIFO for a port data transfer operation. A0–A35 data is written to the mail1 register on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, and MBA is high. B0–B35 data is written to the mail2 register on a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, ENB is high, and MBB is high.

When data is written to a mail register, its mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) is set low. The $\overline{MBF1}$ flag is set high on a low-to-high transition of CLKB when a read is selected for port B and the MBB input is high. The $\overline{MBF2}$ flag is set high on a low-to-high transition of CLKA when a read is selected for port A and the MBA input is high. The data in a mailbox register remains intact after it is read and changes only when new data is written to the register. When a port's data output registers are active, a high on the mailbox enable (MBA or MBB) selects mail data to be output on the port, and a low selects FIFO data for output.

### reset

The FIFO memories of the SN74ACT7822 are reset separately by taking their reset inputs ($\overline{RST1}$ or $\overline{RST2}$) low for at least four CLKA and four CLKB low-to-high transitions. The reset inputs may be asynchronous with respect to either clock. This resets the internal read and write pointers to their initial locations and forces the FIFOs' $\overline{AF}$ flags high and IR, OR, and $\overline{AE}$ flags low. Resetting a FIFO also forces the flag of its parallel mailbox register high. Data outputs of the FIFO and mailbox register are not reset to any specific logic level. Both FIFOs must be reset upon power up.

PRODUCT PREVIEW

### almost full and almost empty flags

Three preset values are available for the offsets of the almost full and almost empty flags of a FIFO, or values can be programmed for each flag from port A. The flag select inputs (FS0, FS1) are sampled for each FIFO by the low-to-high transition of its reset input. If the values of FS0 and FS1 select a flag default value at the time of the rising edge of $\overline{RST1}$ or $\overline{RST2}$, the default value is set as the offset for the almost full and almost empty flags of the FIFO.

To program the almost full and almost empty flags of FIFO1 and FIFO2, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset signals. After this reset cycle, IRA is forced high on the second low-to-high transition of CLKA, but IRB remains low until the programming is complete. The first four writes to FIFO1 program offsets for flags in the order of $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$ and $\overline{AFB}$. The offsets may be programmed from 1 to 508. The IRB flag is asserted high by the second CLKB low-to-high transition after the $\overline{AFB}$ offset is programmed. The fifth write to FIFO1 stores the first word in its memory array.

An almost empty flag is low when the number of 36-bit words stored in its FIFO is less than or equal to the flag's offset value. An almost full flag is low when the number of empty locations left in its FIFO is less than or equal to the flag's offset value. Data in the output register of a FIFO has been read from memory, and its previous location is free.

**FLAG PROGRAMMING TABLE**

| FS1 | FS0 | $\overline{RST1}$ | $\overline{RST2}$ | FIFO1 OFFSET | FIFO2 OFFSET |
|---|---|---|---|---|---|
| H | H | ↑ | X | 64 | X |
| H | H | X | ↑ | X | 64 |
| H | L | ↑ | X | 16 | X |
| H | L | X | ↑ | X | 16 |
| L | H | ↑ | X | 8 | X |
| L | H | X | ↑ | X | 8 |
| L | L | ↑ | ↑ | Programmed from port A | Programmed from port A |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage, $V_I$ ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −4 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = − 4 mA | | 2.4 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | | ±5 | μA |
| $I_{OZ}$ | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | | ±5 | μA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$§ | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | $V_I$ = 0, | f = 1 MHz | | | 4 | | pF |
| $C_o$ | $V_O$ = 0, | f = 1 MHz | | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

PRODUCT PREVIEW

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 30 pF (unless otherwise noted)**

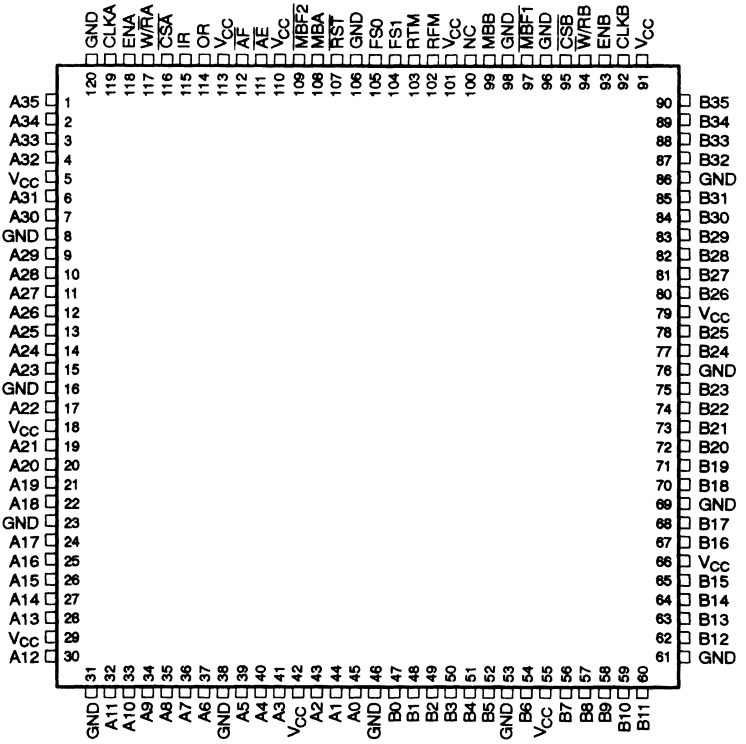
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7822-15 | | 'ACT7822-20 | | 'ACT7822-25 | | 'ACT7822-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKA or CLKB | | 67 | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | CLKA↑ | A0–A35 | | 12 | | 13 | | 15 | | 17 | ns |
| | CLKB↑ | B0–B35 | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | IRA | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | IRB | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | ORA | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | ORB | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | $\overline{AFA}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | $\overline{AFB}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | $\overline{AEA}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | $\overline{AEB}$ | | 12 | | 13 | | 15 | | 17 | |
| $t_{PHL}$ | CLKA↑ | $\overline{MBF1}$ | | 11 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKB↑ | | | 11 | | 12 | | 14 | | 16 | |
| $t_{PHL}$ | CLKB↑ | $\overline{MBF2}$ | | 11 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKA↑ | | | 11 | | 12 | | 14 | | 16 | |
| $t_{pd}$ | MBA | A0–A35 | | 11 | | 12 | | 14 | | 16 | ns |
| | MBB | B0–B35 | | 11 | | 12 | | 14 | | 16 | |
| $t_{PHL}$ | $\overline{RST1}$ | $\overline{AEB}$ | | | | | | | | | ns |
| | $\overline{RST2}$ | $\overline{AEA}$ | | | | | | | | | |
| $t_{PLH}$ | $\overline{RST1}$ | $\overline{AFA}$ | | | | | | | | | ns |
| | $\overline{RST2}$ | $\overline{AFB}$ | | | | | | | | | |
| $t_{PLH}$ | $\overline{RST1}$ | $\overline{MBF1}$ | | | | | | | | | ns |
| | $\overline{RST2}$ | $\overline{MBF2}$ | | | | | | | | | |
| $t_{en}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | | | | | | | | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | | | | | | | | | |
| $t_{dis}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | | | | | | | | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | | | | | | | | | |

PRODUCT PREVIEW

JUNE 1992

- Member of the Texas Instruments *Widebus+*™ Family
- Free-Running CLKA and CLKB May Be Asynchronous or Coincident
- 1024 × 36 Clocked FIFO Buffering Data From Port A to Port B
- Retransmit Capability
- Mailbox Register in Each Direction
- Programmable Almost Full and Almost Empty Flags
- Microprocessor Interface Control Logic
- IR and $\overline{AF}$ Flags Synchronized by CLKA
- OR and $\overline{AE}$ Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 12 ns
- Available in 132-Pin Quad Flatpack (PQ) or Space-Saving 120-Pin Shrink Quad Flatpack (PCB)

PCB PACKAGE
(TOP VIEW)




NC – No internal connection

Widebus+ is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

JUNE 1992

## description

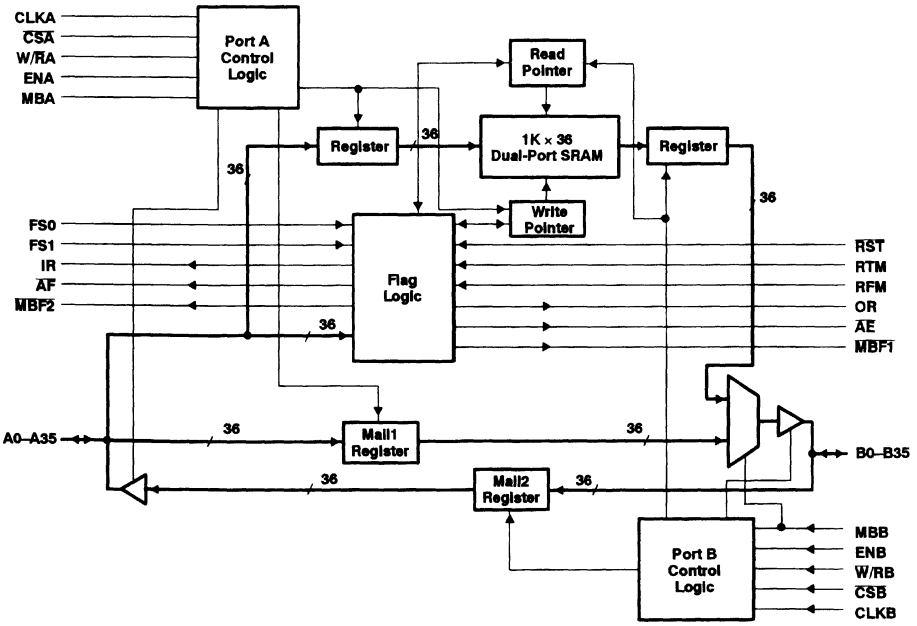
The SN74ACT7823 is a high-speed, low-power CMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12 ns. The 1024 x 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port may take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices may be used in parallel to create wider data paths.

The SN74ACT7823 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input ready flag (IR) and almost full flag ($\overline{AF}$) of the FIFO are two-stage synchronized to CLKA. The output ready flag (OR) and almost empty flag ($\overline{AE}$) of the FIFO are two-stage synchronized to CLKB. Offsets for the almost full and almost empty flags of the FIFO can be programmed from port A.

PRODUCT PREVIEW

## functional block diagram



### FIFO function

The state of the A0–A35 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to the FIFO on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, MBA is low, ENA is high, and the IR flag is high.

The state of the B0–B35 outputs is controlled by $\overline{CSB}$ and $\overline{W}$/RB. When $\overline{CSB}$ is low and $\overline{W}$/R B is high, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. Data is read from the FIFO to the B0–B35 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is high, MBB is low, ENB is high, and the ORB flag is high.

The setup and hold time constraints to the port clocks for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, $\overline{W}$/RB) are for enabling write and read operations and are not related to high-impedance control of the data outputs. If the master enable signal for a port (ENA or ENB) is set low during a clock cycle, the chip select and read/write select may switch at any time during the cycle to change the state of the data outputs.

Each FIFO flag is two-stage synchronized to a port clock for use as a reliable synchronous control signal. CLKA synchronizes the status of the input ready flag (IR) and almost full flag ($\overline{AF}$) of the FIFO. CLKB synchronizes the status of the output ready flag (OR) and almost empty flag ($\overline{AE}$) of the FIFO.

When the input ready flag is low, the FIFO is full, and writes are disabled to its array. When the output ready flag is low, the FIFO is empty, and reads from memory are disabled. The first word loaded to an empty memory is sent to the FIFO's output register when the output ready flag is asserted (high). When the memory is read empty and the output ready flag is forced low, the last valid data remains on the FIFO outputs until the output ready flag is asserted (high) again. In this way, a high on the output ready flag indicates that new data is present on the FIFO outputs.

### mailbox registers

Bidirectional communication between ports may take place through the mailbox registers. The mailbox-select inputs (MBA, MBB) choose between a mail register and a FIFO for a port data transfer operation. A0–A35 data is written to the mail1 register on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, and MBA is high. B0–B35 data is written to the mail2 register on a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, ENB is high, and MBB is high.

When data is written to a mail register, its mailbox register flag ($\overline{MBF1}$, $\overline{MBF2}$) is set low. The $\overline{MBF1}$ flag is set high on the low-to-high transition of CLKB when a read is selected for port B and the MBB input is high. The $\overline{MBF2}$ flag is set high on the low-to-high transition of CLKA when a read is selected for port A and the MBA input is high. The data in a mailbox register remains intact after it is read and changes only when new data is written to the register. When the data outputs of port B are active, a high on MBB selects mail1 data to be output on the port, and a low selects FIFO data for output.

### reset

The SN74ACT7823 is reset by taking the reset input ($\overline{RST}$) low for at least four CLKA and four CLKB low-to-high transitions. The reset input may be asynchronous with respect to either clock. This resets the internal read and write pointers to the initial location and forces the FIFO's $\overline{AF}$ flag high and IR, OR, and $\overline{AE}$ flags low. Resetting the device also forces the mailbox register flags ($\overline{MBF1}$, $\overline{MBF2}$) high. Data outputs of the FIFO and mailbox registers are not reset to any specific logic level. The device must be reset upon power up.

PRODUCT PREVIEW

### almost full and almost empty flags

Three preset values are available for the offsets of the almost full and almost empty flags, or offsets can be programmed for each flag from port A. The flag select inputs (FS0, FS1) are sampled by the low-to-high transition of the reset input. If the values on FS0 and FS1 select a flag preset value at the time of the rising edge of $\overline{RST}$, the preset value is set as the offset for the almost full and almost empty flags (see flag programming table).

To program the almost full and almost empty flags from port A, the flag select inputs must be low during the low-to-high transition of the reset signal. After this reset cycle, the first write to the FIFO programs the $\overline{AE}$ offset, and the second write programs the $\overline{AF}$ offset. Flag offset values may be programmed from 1 to 1000. The third write to the FIFO stores the first word in its memory array.

The almost empty flag is low when the number of 36-bit words stored in the FIFO is less than or equal to the flag's offset value. An almost full flag is low when the number of empty locations left in the FIFO is less than or equal to the flag's offset value. Data in the output register of the FIFO has been read from memory, and its previous location is free.

**FLAG PROGRAMMING TABLE**

| FS1 | FS0 | $\overline{RST}$ | $\overline{AF}$ and $\overline{AE}$ |
|---|---|---|---|
| H | H | ↑ | 64 |
| H | L | ↑ | 16 |
| L | H | ↑ | 8 |
| L | L | ↑ | Programmed from port A |

### retransmit

A selected portion of data in the FIFO may be read repeatedly when it is put in retransmit mode. The FIFO is put in retransmit mode by asserting the retransmit mode input (RTM) high during a low-to-high transition of CLKB. If valid data is present on the bus at this time, it is the first data to be output when retransmit is activated. The FIFO is in retransmit mode until RTM is low during a low-to-high transition of CLKB. While the FIFO is in retransmit mode, it is filled by the 1024th word written after the first retransmit data.

When the FIFO is in the retransmit mode, a high level on the RFM input enables a low-to-high transition of CLKB to begin a retransmit. This clock edge resets the read pointer to the first retransmit location and outputs the first retransmit data. Data may be retransmitted from the selected starting position repeatedly. A new retransmit starting position is selected after taking the FIFO out of retransmit mode by putting the device in retransmit mode again.

## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A35 | I/O | Port A data. 36-bit bidirectional data port for side A. |
| $\overline{AE}$ | O | Almost empty flag. Programmable flag synchronized to CLKB. It is low when the number of words in the FIFO is less than or equal to the selected value. |
| $\overline{AF}$ | O | Almost full flag. Programmable flag synchronized to CLKA. It is low when the number of empty locations in the FIFO is less than or equal to the selected value. |
| B0–B35 | I/O | Port B data. 36-bit bidirectional data port for side B. |
| CLKA | I | Port A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and may be asynchronous or coincident to CLKB. IR and $\overline{AF}$ are synchronous to the low-to-high transition of CLKA. |
| CLKB | I | Port B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and may be asynchronous or coincident to CLKA. OR and $\overline{AE}$ are synchronous to the low-to-high transition of CLKB. |
| $\overline{CSA}$ | I | Port A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high. |
| $\overline{CSB}$ | I | Port B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high. |
| ENA | I | Port A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A. |
| ENB | I | Port B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B. |
| FS1, FS0 | I | Flag offset selects. The low-to-high transition of $\overline{RST}$ latches the states of FS0 and FS1. If either FS0 or FS1 is high when the reset input goes high, one of three preset values is selected as the offset for the almost full and almost empty flags. If both FS0 and FS1 are low when $\overline{RST}$ goes high, the first two writes to the FIFO program the almost full and almost empty offsets. |
| IR | O | Input ready flag. IR is synchronized to the low-to-high transition of CLKA. When IR is low, the FIFO is full, and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set low during reset and is set high on the second low-to-high transition of CLKA after reset. |
| MBA | I | Port A mailbox select. A high level chooses a mailbox register for a port A read or write operation. |
| MBB | I | Port B mailbox select. A high level chooses a mailbox register for a port B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output, and a low level selects FIFO data for output. |
| $\overline{MBF1}$ | O | Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port B read is selected and MBB is high. $\overline{MBF1}$ is set high by a reset. |
| $\overline{MBF2}$ | O | Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port A read is selected and MBA is high. $\overline{MBF2}$ is set high by a reset. |
| OR | O | Output ready flag. OR is synchronized to the low-to-high transition of CLKB. When OR is low, the FIFO is empty, and reads are disabled. Ready data is present on the output register of the FIFO when OR is high. OR is forced low during the reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory. |
| RFM | I | Read from mark. When the FIFO is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the read pointer to the retransmit location and output the first selected retransmit data. |
| $\overline{RST}$ | I | Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST}$ is low. The low-to-high transition of $\overline{RST}$ latches the status of FS0 and FS1 for $\overline{AF}$ and $\overline{AE}$ offset selection. |
| RTM | I | FIFO retransmit mode. When RTM is high and valid data is present on the output of the FIFO, a low-to-high transition of CLKB selects the data for the beginning of a retransmit. The selected position remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, which takes the FIFO out of retransmit mode. |
| W/$\overline{R}$A | I | Port A write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{R}$A is high. |
| $\overline{W}$/RB | I | Port B $\overline{write}$/read select. A low selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{W}$/RB is low. |

PRODUCT PREVIEW

## recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −4 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −4 mA | | 2.4 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | | | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or 0 | | | | ±5 | μA |
| $I_{OZ}$ | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or 0 | | | | ±5 | μA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ − 0.2 V or 0 | | | | 400 | μA |
| $\Delta I_{CC}$‡ | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 1 | mA |
| $C_i$ | $V_I$ = 0, | f = 1 MHz | | | 4 | | pF |
| $C_o$ | $V_O$ = 0, | f = 1 MHz | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or $V_{CC}$.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 30 pF (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7823-15 | | 'ACT7823-20 | | 'ACT7823-25 | | 'ACT7823-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKA or CLKB | | 67 | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | CLKB↑ | B0–B35 | | 12 | | 13 | | 15 | | 17 | ns |
| | CLKA↑ | $\overline{IR}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | $\overline{OR}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKA↑ | $\overline{AF}$ | | 12 | | 13 | | 15 | | 17 | |
| | CLKB↑ | $\overline{AE}$ | | 12 | | 13 | | 15 | | 17 | |
| $t_{PHL}$ | CLKA↑ | $\overline{MBF1}$ | | 11 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKB↑ | | | 11 | | 12 | | 14 | | 16 | |
| $t_{PHL}$ | CLKB↑ | $\overline{MBF2}$ | | 11 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKA↑ | | | 11 | | 12 | | 14 | | 16 | |
| $t_{pd}$ | MBB | B0–B35 | 11 | | 12 | | 14 | | 16 | | ns |
| $t_{PHL}$ | $\overline{RST}$ | $\overline{AE}$ | | | | | | | | | ns |
| $t_{PLH}$ | $\overline{RST}$ | $\overline{AF}$ | | | | | | | | | ns |
| | | $\overline{MBF1}$, $\overline{MBF2}$ | | | | | | | | | |
| $t_{en}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | 10 | | 11 | | 12 | | 13 | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | 10 | | 11 | | 12 | | 13 | | |
| $t_{dis}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | 10 | | 11 | | 12 | | 13 | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | 10 | | 11 | | 12 | | 13 | | |

PRODUCT PREVIEW

# 64-Byte FIFOs
# SN74ALS2232A and SN74ALS2233A

## First-In, First-Out Technology

**Kam Kittrell**
**General Purpose Logic — Semiconductor Group**
**Texas Instruments**

TEXAS INSTRUMENTS

## 64-Byte FIFOs
## SN74ALS2232A and SN74ALS2233A

### Introduction

First-In, First-Out memories (FIFOs) are irreplaceable bus logic when interfacing two asynchronous systems or controlling data flow paths. The SN74ALS2232A 64 x 8 and SN74ALS2233A 64 x 9 FIFOs from Texas Instruments offer high-performance buffering for shallow-word-depth applications. These devices are produced in TI's IMPACT-X bipolar technology and are packaged in 24- or 28-pin DIP and 28-pin PLCC.

### Clocking

The SN74ALS2232A and SN74ALS2233A FIFOs are organized with dual-port SRAM, write addressing, read addressing, and address comparator logic for flag generation. As opposed to shift-register architectures, the dual-port SRAM architecture allows data to pass from the input to the output of an empty FIFO with a minimal delay independent of FIFO depth and also allows high-frequency data transfers.

The load clock (LDCK) and unload clock (UNCK) inputs of a FIFO are low-to-high-edge triggered clocks that initiate memory operations and control addressing increments. By allowing a single clock edge to activate action on the circuit and automating the memory timing and address increment timing, data transfer control is made easy. Only the rising edge of each device clock must be maintained for precise timing, while the falling edge may vary greatly within the cycle without altering performance (see Figure 1). This is a feature of all TI FIFOs with dual-port SRAM architecture.

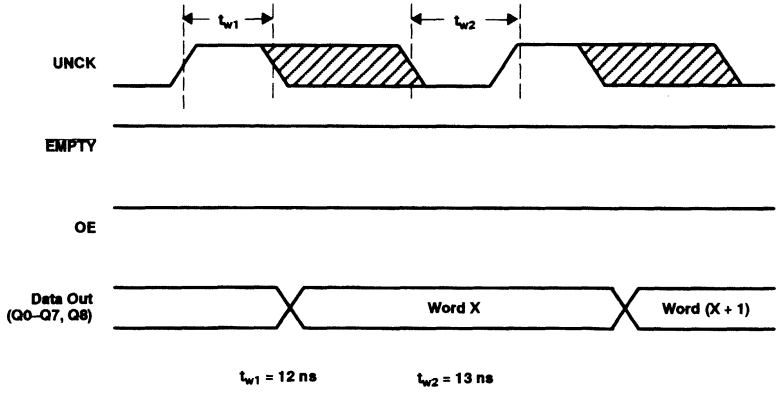



**Figure 1. SN74ALS2232A and SN74ALS2233A Clock Input Circuit**

## Noise Control

Ground bounce is a voltage transient produced by current surges through the ground pin. Due to bond wire, lead, and board parasitic inductance, changes in the ground current will result in a voltage forced on ground. A ground voltage transient peak-to-peak value increases with an increase in the number of outputs switching from high to low, an increase in output load capacitance, and an increase in $V_{CC}$. The chip's ground voltage can also be influenced by following negative undershoot voltages applied to inputs and outputs.

The inputs of a digital device are referenced to its ground. Large voltage transients applied to ground can cause threshold switching by steady-state low or high levels applied to an input. For the SN74ALS2232A and SN74ALS2233A, an unwanted threshold crossing creates the most problems on the rising-edge-triggered clocks, LDCK and UNCK, by generating false clocks. The results of false clocking produced by high ground noise levels can appear as multiple storage of data words, missed data words in a stream, or the inability to empty the device.

By placing the GND pin of the SN74ALS2232A and SN74ALS2233A in the center of the DIP and PLCC packages to employ the shortest bond wire and lead path, package inductance and ground bounce effects are minimized. Ground bounce can be minimized further by decoupling the power planes of the board in close proximity to the device with a capacitor (about 0.1 μF). Undershoot voltages on the inputs and outputs of a device are controlled by eliminating voltage reflections due to transmission line effects.

In an unusually noisy environment such as a wire-wrap prototype wherein it is difficult to control input and output undershoot voltages, generating the LDCK and UNCK inputs as inactive high reduces the possibility of false clocking. Figure 2 shows the one-shot circuit for the LDCK and UNCK inputs. When the input to the one-shot is at a steady-state low logic level, a very quick voltage transient (about 3 to 5 ns) caused by ground noise can trigger a pulse on the one-shot output. A low-noise pulse of the same duration is less likely to pass through the circuit if the input is at a steady-state high logic level.

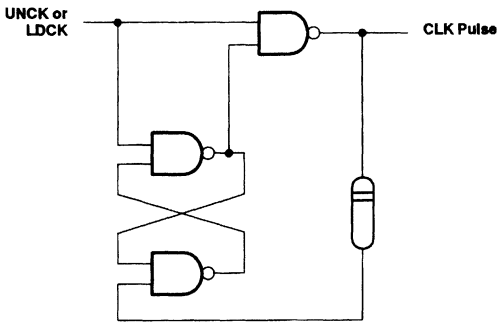



**Figure 2. SN74ALS2232A and SN74ALS2233A Clock Input Circuit**

## Applications

### FIFO Flags

The $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ flags are provided to indicate FIFO boundary conditions and prevent overflow and underflow conditions from occurring. The flags are the outputs of a circuit that compares the write and read addresses of the dual-port SRAM. In cases where the LDCK and UNCK inputs operate asynchronously to each other, these signals are useful for read and write control after synchronization. Figure 3 is an example of flag synchronization for clock control. The $\overline{\text{FULL}}$ flag is synchronized to LDCK to indicate when the device has exited a full state and prevent additional memory write attempts when is is filled again. Likewise, the $\overline{\text{EMPTY}}$ flag is synchronized to UNCK to indicate when the device is no longer empty and prevent memory read attempts when it is empty.

In addition to the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ flags, the SN74ALS2233A also has a HALF-FULL flag that is high when 32 or more words are contained in memory and an AF/AE flag (almost full/almost empty) that is high when eight or less locations in memory are filled or eight or less empty locations are available. These flags are useful for signaling when blocks of data may be transferred through the FIFO in consecutive clock cycles.

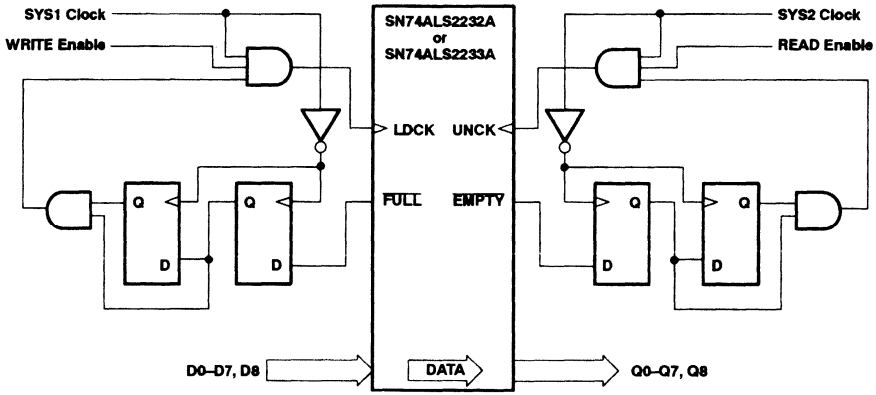



**Figure 3. Clock Generation With Two-Stage Synchronization of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$**

### Bus Conversion

Shallow FIFO memories are often used when data is transferred between a 16- or 32-bit bus to an 8-bit memory or peripheral device. Figure 4 is an example in which two SN74ALS2232A or two SN74ALS2233A devices are used for converting (folding) a 16-bit bus into an 8-bit bus. The three-state outputs of the FIFOs are used to "ping-pong" between devices. This configuration can be expanded using similar control to accomodate a 32-bit input bus with an 8- or 16-bit output bus. The FIFOs allow data to be transferred in burst mode from the input bus without being slowed by the smaller output bus. With the same folding logic designed to control the input of the FIFOs, data may be transferred from an 8- or 16-bit bus and unfolded to a 16- or 32-bit bus.

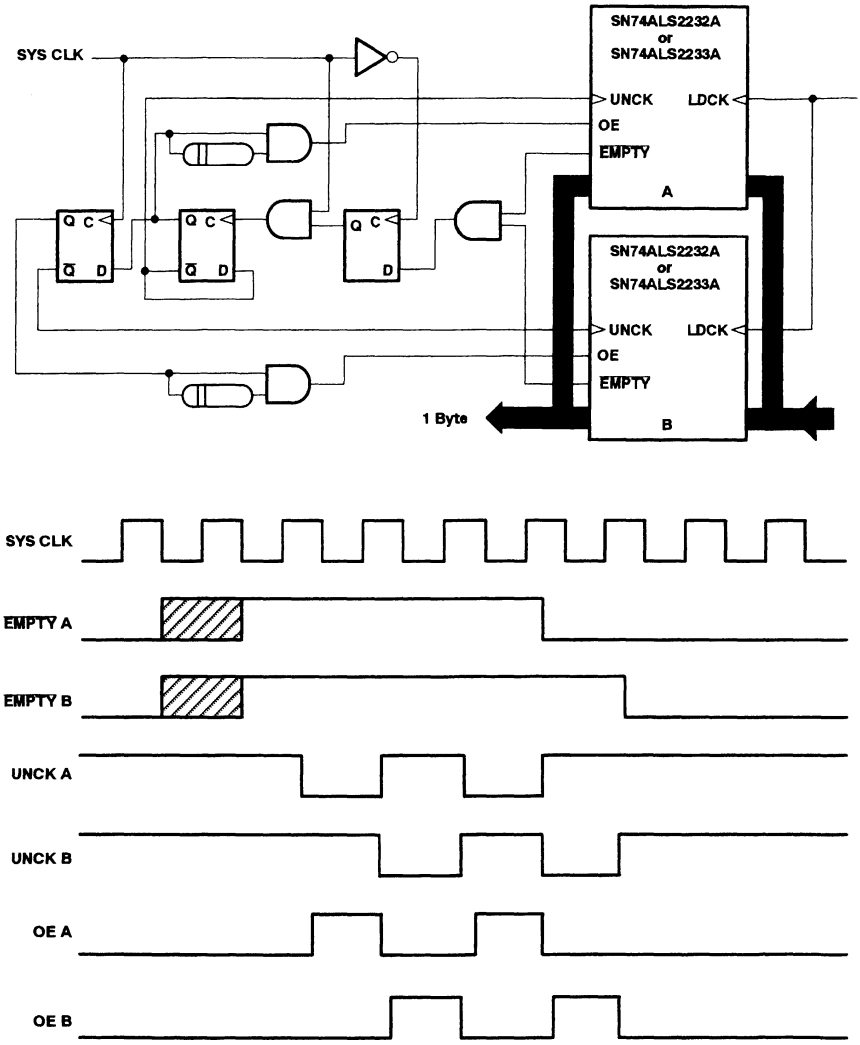



**Figure 4. Bus Folding Logic**

# 1K × 9 × 2 Asynchronous FIFOs SN74ACT2235 and SN74ACT2236

## First-In, First-Out Technology

Kam Kittrell
Semiconductor Group
Texas Instruments

TEXAS INSTRUMENTS

## 1K × 9 × 2 Asynchronous FIFOs
## SN74ACT2235 and SN74ACT2236

### Introduction

Texas Instruments designed the 'ACT2235 to meet a variety of synchronous or asynchronous bidirectional applications. Two 1K × 9 First-In, First-Out (FIFO) memories are arranged in parallel to buffer data in opposite directions. Data ports may also exchange real-time data. Three-state control (GAB, GBA) and real-time/stored data select (SAB, SBA) match the popular '652 transceiver logic. Produced in TI's EPIC CMOS process, the inputs accept TTL voltage levels. An option to the 'ACT2235 is the 'ACT2236, which has '646 transceiver control (DIR, $\overline{G}$).

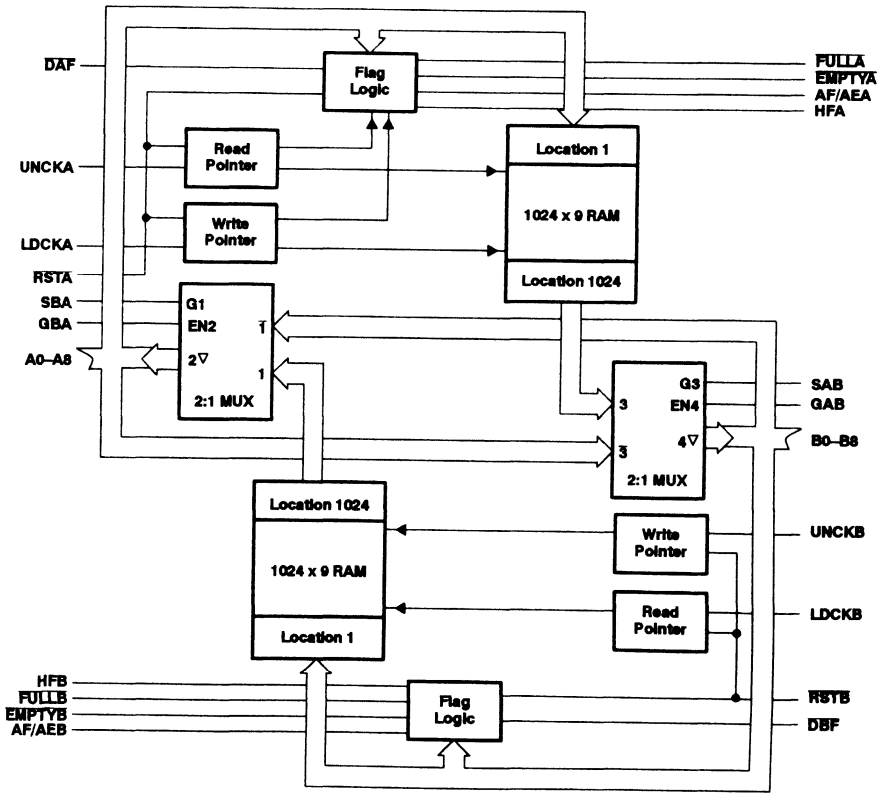
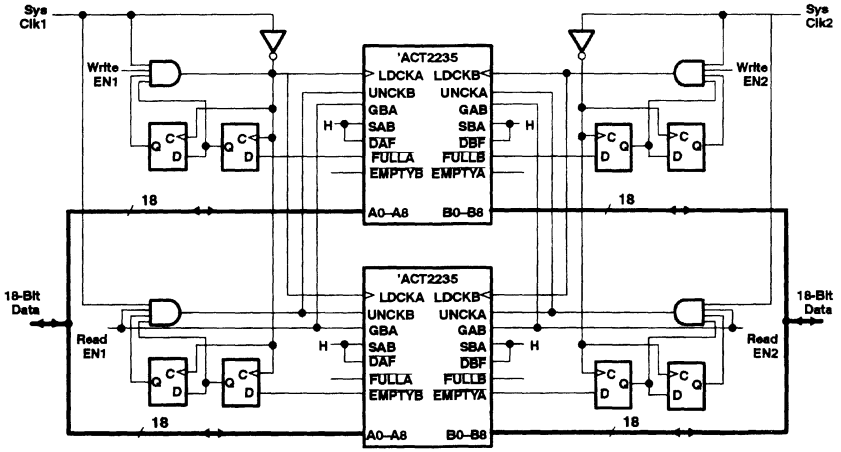



**Figure 1. SN74ACT2235 Block Diagram**

## FIFO Control

The 'ACT2235 consists of two FIFO memories, FIFOA and FIFOB. Both FIFOs can be accessed from either port A or port B. Four control signal lines (GAB, GBA, SAB and SBA) control the eight possible data flow paths through the device (these data paths are illustrated in the device data sheet). Each FIFO has a load clock (LDCK) that writes data into memory and an unload clock (UNCK) that reads the data in the same order it was written. Both clocks are positive-edge-triggered and may operate asynchronously to one another. The first word loaded into an empty FIFO propagates directly to the outputs, and the $\overline{\text{EMPTY}}$ flag switches high. $\overline{\text{EMPTY}}$ represents the valid state of data on the outputs (data is valid when $\overline{\text{EMPTY}}$ is high and invalid when $\overline{\text{EMPTY}}$ is low). $\overline{\text{EMPTY}}$ may be used to enable an UNCK pulse when it is synchronized with the bus that will read the data. $\overline{\text{FULL}}$ can qualify a LDCK pulse in the same way.

Figure 2 is an example of an 'ACT2235 interfacing two asynchronous systems. Each system provides a read enable, write enable, and free-running clock. A flag must be synchronized to the system clock to use it as device clock control. Although the flag's high-to-low transition is synchronous to the clock it enables, the low-to-high transition is asynchronous. The output of the latch qualifying this transition can go metastable when bistable (setup and hold) conditions are not met. An output is metastable if it lingers between the specified $V_{OH}$ and $V_{OL}$ levels. Two-stage synchronization of the flags reduces the probability of a metastable-induced failure.




Note: Two devices are used for 18-bit width expansion.

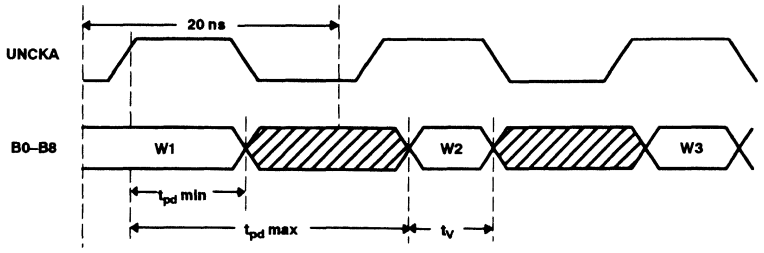
**Figure 2. Controlling the 'ACT2235 Using a Clock, Write Enable, and Read Enable Per System**

## High-Frequency Applications

A unique feature of the 'ACT2235 is that the UNCK cycle time may be less than the device access time. The 'ACT2235–20 has a maximum LDCK and UNCK frequency of 50 MHz (20 ns cycle time) and a 25-ns maximum access time ($t_{pd}$ UNCKA or UNCKB to B bus or A bus). In a series of FIFO reads, the next access may be initiated before the present one is complete. The largest concern associated with this technique is the length of time data will be guaranteed as valid. Minimum access time from the rising edge of UNCK may also be viewed as minimum data hold time on the bus. Timing for this relationship is shown in Figure 3. Valid data time from the 'ACT2235 over the commercial temperature range and ± 10% $V_{CC}$ is given by:

$$t_v = t_{cycle} + t_{pd}\,\text{min} - t_{pd}\,\text{max} \quad (1)$$

Data from an 'ACT2235 operating at a 50-MHz clock frequency is valid for at least 7 ns. This allows a 4-ns setup and 1-ns hold with 2 ns of tolerance to the next device in the data path.




For 'ACT2235–20: $t_{pd}$ min = 12 ns, $t_{pd}$ max = 25 ns, $t_v$ = 7 ns

**Figure 3. Read Operation When Cycle Time Is Less Than Access Time**

## Programmable Flags

Data is often transmitted in packets, where each packet is a specific number of bytes and must be delivered in an unbroken stream. A FIFO transmitting packeted data needs a flag that shows the number of bytes stored. This keeps from breaking the transmission of a packet due to an empty or full condition. The 'ACT2235 has a programmable almost full/almost empty flag for this application. The AF/AEA offset value (X) and the AF/AEB offset value (Y) are programmed separately. AF/AEA is high when FIFOA contains X or fewer words or (1024 minus X) or more words. It is low when FIFOA contains between (X + 1) and (1023 minus X) words. AF/AEB functions in the same manner with its programmed value, Y. The programmed or default value of 256 is chosen during a reset of each FIFO.

The device's internal flag programming logic is illustrated in Figure 4. Programming the AF/AE flag value for each FIFO is done with the define flag inputs ($\overline{DAF}$, $\overline{DBF}$) and resets ($\overline{RSTA}$, $\overline{RSTB}$). Define flag inputs are negative-edge-triggered clocks that store input data to a register. If $\overline{DAF}$ or $\overline{DBF}$ is low when the rising edge of $\overline{RSTA}$ or $\overline{RSTB}$ occurs, the registered value is used for the FIFO's AF/AE flag. The flag uses the default value of 256 if $\overline{DAF}$ or $\overline{DBF}$ is high during the rising edge of $\overline{RSTA}$ or $\overline{RSTB}$.

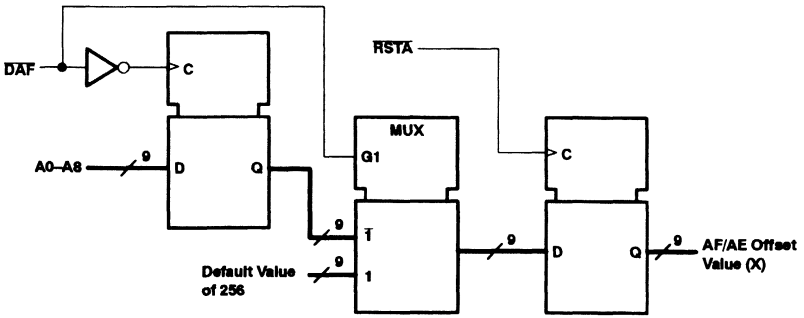



**Figure 4. AF/AEA Flag Programming Logic for FIFOA**

Programming both flag offset values from one port is possible using real-time select. Figure 5 is a timing example of programming AF/AEB from port A. To program the AF/AEB offset value (Y) from port A, the binary value for Y is on A0–A8, SAB is low, and GAB is high. With this configuration, the port A data appears on the inputs of FIFOB, and a falling edge of $\overline{DBF}$ stores the Y value.

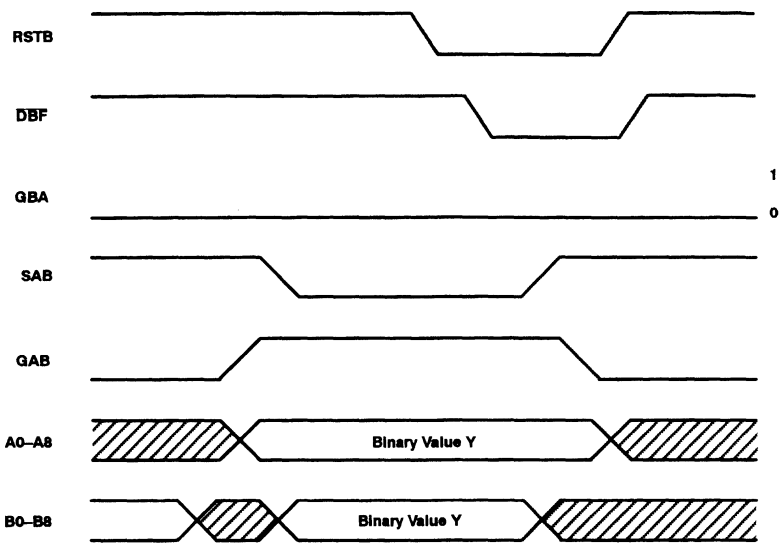



**Figure 5. Programming AF/AEB Flag of FIFOB From Port A**

## Output Drive

Charging and discharging the load of a bus with acceptable speed requires high device output drive. The I/O ports of the 'ACT2235 provide a 16-mA $I_{OL}$ and an 8-mA $I_{OH}$ for this task.

Most memory devices have low drive capability and require buffers to interface to a bus. Large output transistors that support high current are not used because in doing so, the rate of change of current with respect to time (di/dt) increases. When several outputs switch high or low simultaneously, the rate of change of current through ground and $V_{CC}$ lines multiplies. Voltage transients on the power lines are given by:

$$v = -L \times di/dt \quad (2)$$

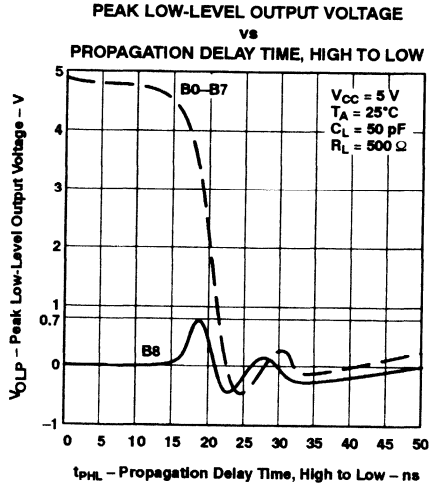
where L equals the inductance of the bond wire and package lead.

The 'ACT2235 provides a twofold solution to allow high output current capability for quickly charging and discharging bus loads with low noise. One solution is to reduce the inductance of ground and $V_{CC}$ lines. The 'ACT2235 has four GND and two $V_{CC}$ pins in parallel. The resulting ground inductance is about 1/4 that of a single connection, and $V_{CC}$ inductance is divided in half.

Reducing di/dt per output transistor is another way to minimize voltage transients. TI's patented Output Edge Control (OEC) design divides a large transistor into smaller segments that turn on in series and turn off simultaneously. OEC lowers di/dt, maintains a quick voltage transition through threshold, and avoids the high power consumed when gradually turned off .[1]

The result of a $V_{OLP}$ test on the 'ACT2235 is shown in Figure 6. $V_{OLP}$ is a measurement of ground voltage noise when all outputs of a bus are switched from high to low. Eight of nine outputs of a bus are switched, and the peak voltage rise of the steady-state low output is measured. Maximum ground voltage rise is only 700 mV. Also note that the output fall time is less than 3 ns with a 50-pF load.

[1] Advanced CMOS Logic Designer's Handbook, pages 3-1 through 3-12




Note: 8 bus outputs switching; 1 remains low

**Figure 6**

## Conclusion

The 'ACT2235 and 'ACT2236 provide several advantages for high-speed asynchronous bus interfacing. Simple control logic offers great design flexibility. Programmable flags may be used for data flow optimization. High output drive for bus loading is balanced with noise reduction through package and circuit design.

# FIFO Solutions for Increasing Clock Rates and Data Widths

## First-In, First-Out Technology

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TEXAS INSTRUMENTS

# FIFO Solutions for Increasing Clock Rates and Data Widths

## Introduction

Steady increases in microprocessor operating frequencies and bus widths over recent years have challenged system designers to find FIFO memories that meet their needs. To assist the designer, new FIFOs from Texas Instruments are available with features that complement these microprocessor trends.

Higher data transfer rates have dictated the need for FIFOs to evolve into *clocked* architecture wherein data is moved in and out of the device with synchronous controls. Each synchronous control of the clocked FIFO uses enable signals that synchronize the data exchange to a *free-running* (continuous clock).

Since the continuous clocks on each port of a clocked FIFO may operate asynchronously to each other, internal status signals indicating when the FIFO is empty or full can change with respect to either clock. To use a status signal for port control, it is synchronized to the port's clock on a clocked FIFO. Synchronization of these signals with flip-flops introduces metastability failures that increase with clock frequency. Texas Instruments uses two-stage flag synchronization to greatly improve reliability.

Higher clock frequencies augment raw speed, but greater bandwidth is also achieved by increasing the data width. Wider data paths can have the associated cost of large board area due to increased package sizes. New compact packages for TI's FIFOs reduce this cost.

## Clocked FIFOs

Clocked FIFOs have become popular for relieving bottlenecks in high-speed data traffic. Data transfers for many systems are synchronized to a central clock with read and write enables. These free-running clocks may be input directly to a clocked FIFO with the same enables controlling its data transfer on the low-to-high transition of the clock.

Reducing the number of clocks keeps the interface simple and easy to manage. Extra logic is needed to produce a gated pulse when using a FIFO that accepts a clock only for a data transfer request. The generated clock signal is a derivative of the master clock with a margin of timing uncertainty. At high clock frequencies, this timing uncertainty is not tolerable, and costly adjustments are needed.

Additional logic is also conserved by implementing flag synchronization on the clocked FIFO. Tracking is done to generate flags that indicate when the memory is empty or full. In many applications, the input and output to the FIFO are asynchronous, and the flag signals must be synchronized for use as control. A read will not be completed on the FIFO if no data is ready, so the $\overline{\text{EMPTY}}$ signal is synchronized to the read clock. This synchronous output ready flag (OR) is useful for controlling read operations. Likewise, the $\overline{\text{FULL}}$ signal is synchronized to the write clock, producing the input ready flag (IR).

## Flag Synchronization

As previously explained, one of the advantages of the clocked FIFO is the on-board synchronization of the $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ status flags when the input and output are asynchronous. In one method of synchronization, a single flip-flop captures the asynchronous flag's value (see Figure 1). With this method, the rising transition of data may violate the flip-flop's set-up time and produce a metastable event (metastability is a malfunction of a flip-flop wherein the latch hangs between high and low states for an indefinite period of time).

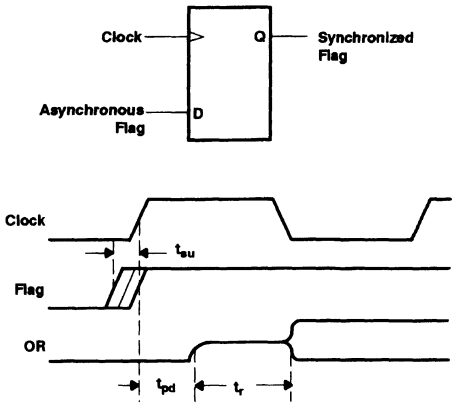



**Figure 1. Triggering a Metastable Event With a One-Stage Synchronizer**

Once a metastable event is triggered, the probability of the output recovering to a high or low level increases exponentially with increased resolve time ($t_r$). The expected time until the output of a single flip-flop with asynchronous data has a metastable event that lasts $t_r$ or longer is characterized by the following mean time between failures (MTBF) equation:

$$MTBF_1 = \frac{\exp\left(\frac{t_r}{\tau}\right)}{t_o f_c f_d}$$

where

$t_o$ = flip-flop constant representing the time window during which changing data will invoke a failure
$t_r$ = resolve time allowed in excess of the normal propagation delay
$\tau$ = flip-flop constant related to the settling time of a metastable event
$f_c$ = clock frequency
$f_d$ = asynchronous data frequency. For OR flag analysis, it is the frequency at which data is written to empty memory. For IR flag analysis, it is the frequency at which data is read from full memory.

The MTBF decreases as clock and data frequency increase and as the time allowed for a metastable event to settle ($t_r$) decreases.

Metastability failures are a formidable issue for short clock cycle times. Increasing the clock frequency linearly increases the number of metastable events triggered, but the shortened available resolve time exponentially increases the the failure rate. It is impossible to eliminate the possibility of a metastable event under these conditions, but solutions exist to reliably increase the expected time between failures.

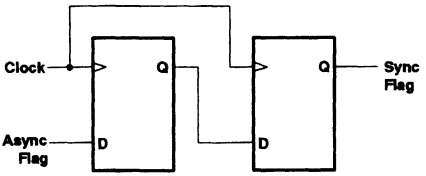


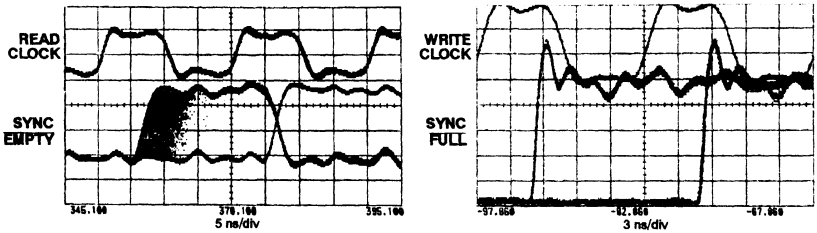

**Figure 2. Two-Stage Synchronizer**

Texas Instruments increases the metastable MTBF by several orders of magnitude for IR and OR flags by employing two-stage synchronization (see Figure 2). For the output of the second stage to be metastable, the first stage must have a metastable event that lingers until it encroaches upon the setup time of the second stage. Adding another stage to a single flip-flop synchronizer is statistically equivalent to increasing its resolve time by the clock period minus its propagation delay. The mean time between failures for a two-stage synchronizer is given by:

$$MTBF_2 = \frac{\exp\left[\frac{t_r + \frac{1}{f_c} - t_p}{\tau}\right]}{t_o f_c f_d}$$

where

$t_p$ = propagation delay of the first flip-flop.




$f_c$ = 50 MHz $f_d$ = 5 MHz $V_{CC}$ = 5 V
(a) ONE-STAGE SYNCHRONIZATION

$f_c$ = 66.7 MHz $f_d$ = 6.7 MHz $V_{CC}$ = 5 V
(b) TWO-STAGE SYNCHRONIZATION

**Figure 3. Storage Oscilloscope Plots Taken Over a 15-Hour Duration**

Figure 3 compares the two synchronization methods discussed. Both plots were taken at room temperature and nominal $V_{CC}$ while each data transition violated set-up time. Figure 3(a) shows the performance of an $\overline{\text{EMPTY}}$ flag synchronizer using only one flip-flop, while Figure 3(b) is the IR flag of an SN74ACT7807 with the write clock operating at maximum frequency.

## Compact Packaging

Microprocessor bus widths have continuously doubled every few years to maximize their performance. Bus widths of 32 and 64 bits are commonplace today, whereas they were almost unheard of a few years ago. The downside to the increased bit count is that each subordinate device in the system must match this width with corresponding increases in board size.

New shrink packages for TI's clocked FIFOs provide a solution to this problem. Multiple-byte data paths can be buffered while covering only a fraction of the area of conventional packages. These new FIFO packages are presently available in 56-, 64-, and 80-pin configurations. Dubbed shrink quad flat pack (SQFP), the 64-pin package is used for 9-bit-wide FIFOs, and the 80-pin package is used for 18-bit-wide FIFOs. Both SQFP packages have a lead pitch of 0.5 mm. The 56-pin shrink small-outline package has a 0.025-inch lead pitch and also houses 18-bit-wide FIFOs. A variety of TI's FIFOs are offered in these new packages (see Table 1).

**Table 1. FIFOs Available In Space-Efficient Packages**

| DEVICE | CLOCKED | ORGANIZATION | CLOCK CYCLE TIME (ns) | PACKAGES |
|---|---|---|---|---|
| SN74ACT2235 | No | 1K x 9 x 2 | 20, 30 40, 50 | 64 SQFP<br>44 PLCC |
| SN74ACT7802 | No | 1K x 18 | 25, 40, 60 | 80 SQFP<br>68 PLCC |
| SN74ACT7811 | Yes | 1K x 18 | 15, 18, 20, 25 | 80 SQFP<br>68 PLCC |
| SN74ACT7803<br>SN74ACT7805<br>SN74ACT7813 | Yes | 512 x 18<br>256 x 18<br>64 x 18 | 15, 20, 25, 40 | 56 SSOP |
| SN74ACT7804<br>SN74ACT7806<br>SN74ACT7814 | No | 512 x 18<br>256 x 18<br>64 x 18 | 20, 25, 40 | 56 SSOP |
| SN74ACT7807 | Yes | 2K x 9 | 15, 20, 25, 40 | 64 SQFP<br>44 PLCC |
| SN74ACT7808 | No | 2K x 9 | 20, 25, 30, 40 | 64 SQFP<br>44 PLCC |

Figure 4 compares the space savings of the new compact packages compared to competitive surface-mount solutions. Note that a four-byte path constructed with four clocked FIFOs in 32-pin PLCC packages consumes 1.16 $in^2$, while two 56-pin SSOP packages cover only 0.59 $in^2$.

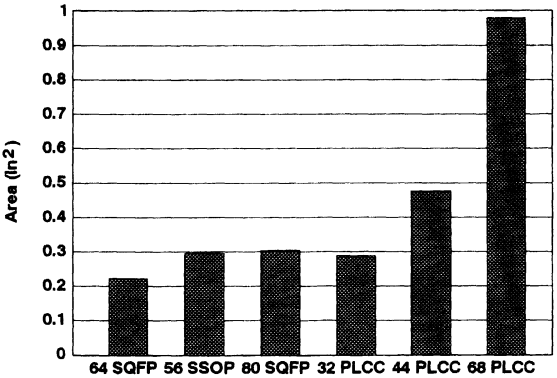



**Figure 4. Surface-Mount Package Area Comparison**

## New Clocked FIFOs

Four new CMOS clocked FIFOs from Texas Instruments offer a variety of memory depths. All four can match applications that require maximum clock frequencies of 67 MHz and access times of 12 ns. Suited for buffering long packets, the 2K x 9 SN74ACT7807 is the deepest of the four and is available in the 44-pin PLCC or 64-pin SQFP. The SN74ACT7803, SN74ACT7805, and SN74ACT7813 are organized as 512 x 18, 256 x 18, and 64 x 18, respectively, and have the same pin arrangement in the 56-pin SSOP. Every TI clocked FIFO is easily expanded in word width, and the SN74ACT7803/05/13 may also be arranged to form a bidirectional FIFO. With the two FIFOs connected as in Figure 1, no extra logic is needed for bidirectional operation.

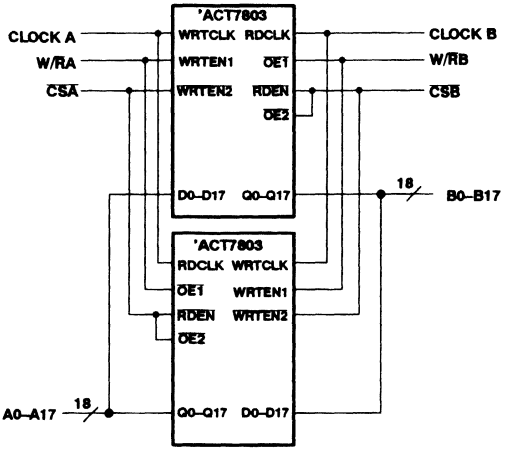



**Figure 5. Bidirectional Configuration for the SN74ACT7803**

Silicon is currently available for a bidirectional clocked FIFO fabricated in TI's Advanced BiCMOS (ABT) process. The SN74ABT7819 is organized as 512 × 18 × 2 with two internal independent FIFOs. Each port has a continuous free-running clock, a chip select ($\overline{CS}$), a read/write select ($\overline{R}/W$), and two separate read and write enables for control. It supports clock frequencies in excess of 80 MHz and a maximum access time below 10 ns. This device will be packaged in the 80-pin QFP and 80-pin SQFP.

## Conclusion

Several semiconductor manufacturers including Texas Instruments have responded to customer needs by providing clocked FIFOs whose synchronous interfaces conform to the requirements of many high-performance systems. Capitalizing on the available continuous system clocks, this architecture limits the amount of necessary glue logic and the number of timing constraints.

Flag synchronization is important for clocked FIFOs buffering between asynchronous systems. Flip-flop synchronizers used for this task have a metastable failure rate that grows exponentially with clock frequency. Texas Instruments employs two stages of synchronization that improve the flags' reliability significantly.

Finally, providing a FIFO buffer for wide buses has historically consumed large amounts of board area. Designers seeking relief from this problem can find it in the packaging options offered for Texas Instruments' FIFOs. Used to house 9- and 18-bit devices, these packages require only about 50% of the space required for conventional surface-mount packages.

# FIFO Surface-Mount Package Information

## FIFO Memory Applications

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# FIFO Surface-Mount Package Information

## Introduction

Texas Instruments provides seven types of plastic surface-mount packages for CMOS FIFO memory devices. These packages and the data bus width that each package can provide are listed in Table 1.

**Table 1. Plastic Surface-Mount FIFO Packages**

| PACKAGE | # OF DATA BITS |
|---|---|
| 44-pin PLCC | 9 |
| 64-pin SQFP | 9 |
| 56-pin SSOP | 18 |
| 68-pin PLCC | 18 |
| 80-pin SQFP | 18 |
| 80-pin QFP | 18 |
| 120-pin SQFP | 32 or 36 |

SSOP = shrink small-outline package
PLCC = plastic leaded chip carrier
SQFP = shrink quad flat pack
QFP = quad flat pack

This application report discusses several topics concerning the FIFO packages listed in Table 1:

- The thermal resistance, $R_{\Theta JA}$, and the chip junction temperature of the device.
- The need for dry packing to maintain safe moisture levels inside the package.
- The three methods used by Texas Instruments for shipping FIFOs to customers.
- The package dimensions, including two-dimensional drawings that show areas, heights, and lead pitches.
- The area comparison of surface-mount packages used for commercial FIFO memories.
- The test sockets available for surface-mount FIFO packages.

## Thermal Resistance

Thermal resistance is defined as the ability of a package to dissipate heat generated by an electronic device and is characterized by $R_{\Theta JA}$. $R_{\Theta JA}$ is the thermal resistance from the IC chip junction to the free air (ambient). Units for this parameter are in degrees Celsius per watt. Table 2 lists $R_{\Theta JA}$ for SSOP, PLCC, SQFP, and QFP packages under five different air flow environments: 0, 100, 200, 250, and 500 linear feet/minute. The chip junction temperature ($T_J$) can be determined using equation 1.

$$T_J = R_{\Theta JA} \times P_T + T_A \quad (1)$$

where

$T_J$ = chip junction temperature (°C)
$R_{\Theta JA}$ = thermal resistance, junction to free-air (°C/watt)
$P_T$ = total power dissipation of the device (watts)
$T_A$ = free-air (ambient) temperature in the particular environment in which the device is operating (°C)

**Table 2. Thermal Resistance, $R_{\Theta JA}$, for FIFO Packages**

| PACKAGE | LEAD FRAME | $R_{\Theta JA}$ (°C/W) | | | | |
|---|---|---|---|---|---|---|
| | | 0 LFPM | 100 LFPM | 200 LFPM | 250 LFPM | 500 LFPM |
| 56-pin SSOP | Copper | 94.2 | 82.2 | N/A | 70 | 57.8 |
| 44-pin PLCC | Copper | 65 | N/A | N/A | N/A | N/A |
| 68-pin PLCC | Copper | 47.2 | 43.4 | N/A | 32.7 | 27.8 |
| 64-pin SQFP | Copper | 92.5 | 87.8 | N/A | 72.9 | 57.8 |
| 80-pin SQFP | Copper | 87.8 | 79.1 | N/A | 67.3 | 54.2 |
| 120-pin SQFP† | Copper | 49.6 | 44.3 | N/A | 38.3 | 28.6 |
| 80-pin QFP | Alloy 42 | 80 | 67 | 61 | N/A | N/A |

† Heat spreader molded inside the package
N/A = not available

Note that $R_{\Theta JA}$ generally increases with decreasing package size; however, this is not true with the 120-pin SQFP package. A heat spreader molded inside the package absorbs a large amount of heat dissipated by the device. As a result, this package provides a relatively low $R_{\Theta JA}$. The 120-pin SQFP is the only package in Table 2 that incorporates a heat spreader.

## Package Moisture Sensitivity

When a plastic surface-mount package is exposed to temperatures typical of furnace reflow, IR (infrared) soldering, or wave soldering (215°C or higher), the moisture absorbed by the package will turn to steam and expand rapidly. The stress caused by this expanding moisture can result in internal and external cracking of the package which can lead to reliability failures. Possible damage includes the delamination of the plastic from the chip surface and lead frame, damaged bonds, cratering beneath the bonds, and external package cracks.

To prevent potential damage, packages that are susceptible to the effects of moisture expansion undergo a process called dry pack. This dry pack process helps to reduce moisture levels inside the package. The process consists of a 24-hour bake at 125°C followed by sealing of the packages in moisture barrier bags with desiccant to prevent reabsorption of moisture during the shipping and storage processes. These moisture barrier bags allow a shelf storage of 12 months from the date of seal. Once the moisture barrier bag is opened, the devices in it must be handled by one of the following four methods, listed in order of preference:

1. The devices may be mounted within 48 hours in an atmospheric environment of less than 60% relative humidity and less than 30°C.
2. The devices may be stored outside the moisture barrier bag in a dry atmospheric environment of less than 20% relative humidity until future use.
3. The devices may be resealed in the moisture barrier bag adding **new** fresh desiccant to the bag. When the bag is opened again, the devices should be used within the 48-hour time limit or resealed again with fresh desiccant.
4. The devices may be resealed in the moisture barrier bag using the **original** desiccant. This method does not allow the floor life of the devices to be extended. The cumulative exposure time before reflow must not exceed a total of 48 hours.

All plastic surface-mount FIFO devices are tested for moisture sensitivity in accordance with Texas Instruments' IPC–SM–786 procedure.

## Shipping Methods/Quantities/Dry Pack

Three methods are used by Texas Instruments for shipping FIFOs to customers. These methods are tubes, tape/reel, and trays. The quantities for each of the shipping methods are listed in Table 3. The shipping quantity is defined as the maximum number of packages that can be packed in a single shipping unit (e.g., the maximum number of 56-pin SSOP packages that can be packed in a tube is 20). Whether or not the packages require dry pack before shipping is denoted by a yes or no in the DRY PACK column.

**Table 3. Shipping Methods and Quantities**

| PACKAGE | SHIPPING METHOD | | | DRY PACK |
|---|---|---|---|---|
| | TUBE† | TAPE/REEL† | TRAYS† | |
| 56-pin SSOP | 20 | 500 | N/A | No |
| 44-pin PLCC | 27 | 500 | N/A | No |
| 68-pin PLCC | 18/19‡ | 250 | N/A | Yes |
| 64-pin SQFP | N/A | N/A | 50 | Yes |
| 80-pin SQFP | N/A | N/A | 50 | Yes |
| 120-pin SQFP | N/A | N/A | 50/84§ | Yes |
| 80-pin SQFP | N/A | N/A | 50 | Yes |

† Texas Instruments reserves the right to change any of the shipping quantities at any time without notice.

‡ 18 packages can be packed in a single tube when pin is used as a tap, or 19 packages can be packed in a tube when plug is used as a tap.

§ Depending on tray size

N/A = not applicable

## Package Dimensions and Area Comparison

Figure 1 contains two-dimensional drawings of the seven available surface-mount FIFO packages. For detailed mechanical drawings of these packages, please refer to the mechanical drawing section of the 1992 *High-Performance FIFO Memories Data Book*.

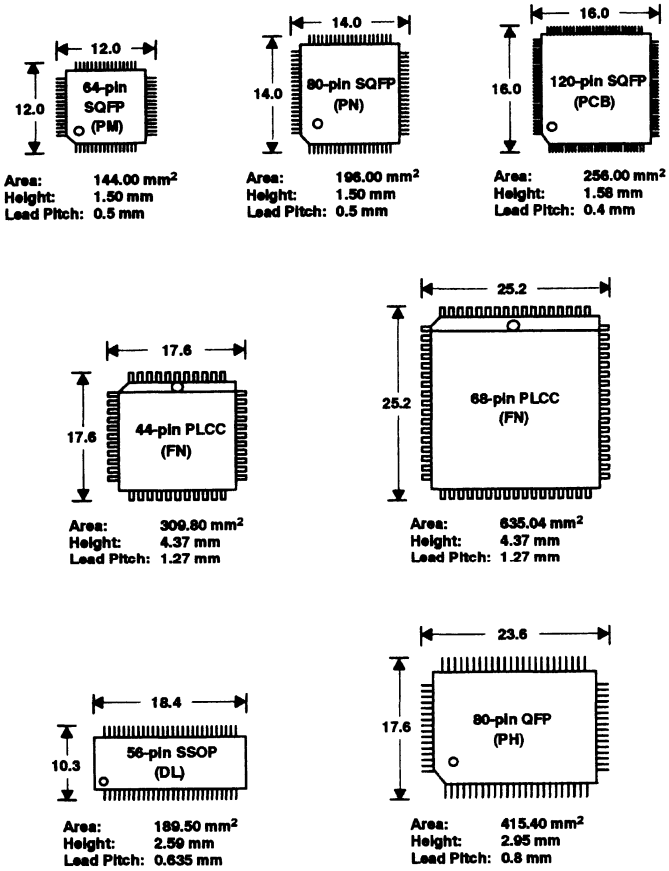



**Figure 1. Package Dimensions**

Figure 2 shows the area comparison of surface-mount packages for FIFOs from Texas Instruments and other FIFO vendors.

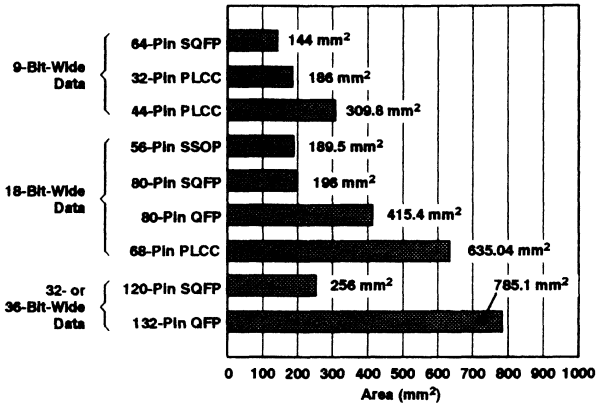



**Figure 2. Surface-Mount Package Area Comparison**

## Test Sockets

For prototype development of a system, it is often an advantage to have sockets for surface-mount products. Test sockets available for use with Texas Instruments' FIFO packages are listed in Table 4. Only one manufacturer is listed for each socket type, although other vendors may offer comparable sockets.

**Table 4. Table 4. Test Sockets for FIFO Packages**

| PACKAGE | MANUFACTURER | NUMBER | DESCRIPTION |
|---|---|---|---|
| 56-pin SSOP | Yamaichi | IC51-0562-1387 | Solder through-hole |
| 44-pin PLCC | NEY | 6044 | Solder through-hole |
| 68-pin PLCC | NEY | 6068 | Solder through-hole |
| 64-pin SQFP | Yamaichi | IC51-0644-807 | Solder through-hole |
| 80-pin SQFP | Yamaichi | IC51-0804-808 | Solder through-hole |
| 120-pin SQFP | Yamaichi | In development (as of 6/92) | Solder through-hole |
| 80-pin QFP | Yamaichi | IC51-0804-394 | Solder through-hole |

# Metastability Performance of Clocked FIFOs

**Author**
**Chris Wellheuser**

TEXAS INSTRUMENTS

# Metastability Performance of Clocked FIFOs

## Introduction

This paper is intended to help the user understand more clearly the issues relating to the metastable performance of Texas Instruments' Clocked FIFOs in asynchronous system applications. It will discuss basic metastable operation theory, show the equations used to calculate metastable failure rates for one and two stages of synchronization, and describe the approach TI has used for synchronizing the status flags on its series of clocked FIFOs. Additionally, a test setup for measuring the failure rate of a device to determine its metastability parameters is shown, and results are given for both an advanced BiCMOS (ABT) FIFO and an advanced CMOS (ACT) FIFO. Using these parameters, calculations of MTBF under varying conditions are performed.

## Metastability

Metastability in digital systems occurs when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state. A common example of this is the case of data violating the setup and hold specifications of a latch or a flip-flop. In a synchronous system, the data will always have a fixed relationship with respect to the clock. As long as that relationship obeys the setup and hold requirements for the device, the output will go to a valid state within its specified propagation delay time. However, in an asynchronous system the relationship between data and clock is not fixed and, therefore, occasional violations of setup and hold times can occur. When this happens, the output may go to an intermediate level between its two valid states and remain there for an indefinite amount of time before resolving itself, or it may simply be delayed before making a normal transition[1]. In either case, a metastable event has occurred.

Metastable events can occur in a system without causing a problem, so it is necessary to define what constitutes a failure before attempting to calculate a failure rate. For a simple CMOS latch, as shown in Figure 1, valid data must be present on the input for a specified period of time before the clock signal arrives (setup time) and must remain valid for a specified period of time with respect to the clock transition (hold time) to guarantee the output will function predictably. This leaves a small window of time with respect to the clock ($t_0$) during which the data is not allowed to change. If a data edge does occur within this aperture, the output may go to an intermediate level and remain there for an indefinite amount of time before resolving itself either high or low, as illustrated in Figure 2. This metastable event can cause a failure only if the output has not resolved itself by the time that it must be valid for use (for example, as an input to another stage). Therefore, the amount of resolve time allowed a device plays a large role in calculating its failure rate.

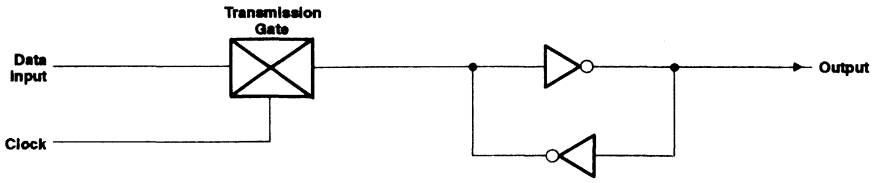



**Figure 1. Simple CMOS Latch**

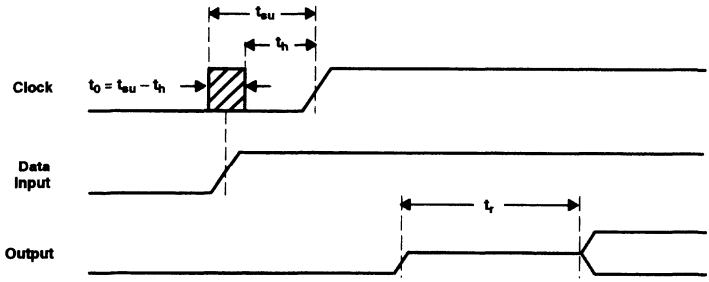



**Figure 2. Output at Intermediate Level Due to Data Edge Within $t_0$ Aperture**

The probability of a metastable state persisting longer than a time $t_r$ decreases exponentially as $t_r$ increases[2]. This relationship can be characterized by the equation

$$F(t_r) = e^{(-t_r/\tau)} \tag{1}$$

where the function $F(t_r)$ is the probability of nonresolution as a function of resolve time allowed, $t_r$, and the circuit time constant $\tau$ (which has also been shown to be inversely proportional to the gain-bandwidth product of the circuit)[3,4].

For a single-stage synchronizer with a given clock frequency and an asynchronous data edge that has a uniform probability density within the clock period, the rate of generation of metastable events can be calculated by taking the ratio of the setup and hold time window described above to the time between clock edges and multiplying by the data edge frequency. This generation rate of metastable events coupled with the probability of nonresolution of an event as a function of the time allowed for resolution gives the failure rate for that set of conditions. The inverse of the failure rate is the mean time between failure (MTBF) of the device and is calculated with the formula shown below:

$$\frac{1}{\text{failure rate}} = \text{MTBF}_1 = \frac{e^{(t_r/\tau)}}{t_0 \, f_c \, f_d} \tag{2}$$

where

- $t_r$ = the resolve time allowed in excess of the normal propagation delay time of the device
- $\tau$ = the metastability time constant for a flip-flop
- $t_0$ = a constant related to the width of the time window or aperture wherein a data edge will trigger a metastable event
- $f_c$ = the clock frequency
- $f_d$ = the asynchronous data edge frequency

The parameters $t_0$ and $\tau$ are constants that are related to the electrical characteristics of the device in question. The simplest way to determine their values is to measure the failure rate of the device under specified conditions and solve for them directly. If the failure rate of a device is measured at different resolve times and plotted, the result is an exponentially decaying curve. When plotted on a semilogarithmic scale, this becomes a straight line the slope of which is equal to $\tau$. Therefore, two data points on the line are sufficient to calculate the value of $\tau$ using the formula below:

$$\tau = \frac{t_{r2} - t_{r1}}{\ln(N1/N2)} \tag{3}$$

where

$t_{r1}$ = resolve time 1
$t_{r2}$ = resolve time 2
N1 = the number of failures relative to $t_{r1}$
N2 = the number of failures relative to $t_{r2}$

After determining the value for $\tau$, $t_0$ may be solved for directly.

The formula for calculating the MTBF of a two-stage synchronizer is merely an extension of equation 1[5]:

$$MTBF_2 = \frac{e^{(t_{r1}/\tau)}}{t_0 f_c f_d} \times e^{(t_{r2}/\tau)} \tag{4}$$

where

$t_{r1}$ = the resolve time allowed for the first stage of the synchronizer
$t_{r2}$ = the resolve time allowed in excess of the normal propagation delay external to the device
$f_c$, $f_d$, $\tau$ and $t_0$ are as defined previously, with $\tau$ and $t_o$ assumed to be the same for both stages

The first term calculates the MTBF of the first stage of the synchronizer, which in effect becomes the generation rate of metastable events for the next stage. The second term then calculates the probability that the metastable event will be resolved based on the value of $t_{r2}$, the resolve time allowed external to the synchronizer. The product of the two terms gives the overall MTBF for the two-stage synchronizer.

## TI Clocked FIFOs

TI's clocked FIFOs are designed to reduce the occurrence of metastable errors due to asynchronous operation. This is achieved through the use of two- and three-stage synchronizing circuits that generate the status flag outputs IR (input ready) and OR (output ready). In a typical application, words may be written to and then read from the FIFO at varying rates independent of one another, resulting in asynchronous flag signal generation (internally) at the boundary conditions of full and empty. For example, consider the operation when the FIFO is at the full boundary condition with writes taking place faster than and asynchronously to reads. The IR flag will be low, signifying that the FIFO is full and can accept no more words. When a read occurs, the FIFO is no longer completely full. This causes an internal flag signal to go high, allowing another write to take place. Since the exit from the full state happens asynchronously to the write clock of the FIFO, this flag is not useful as a system write enable signal. The solution is to synchronize this internal flag to the write

clock through two D-type flip-flop stages and output this synchronized signal as the IR flag (see Figure 3). The OR status flag is generated in a similar manner at the empty boundary condition and is synchronized to the read clock through a three-stage synchronizing circuit.

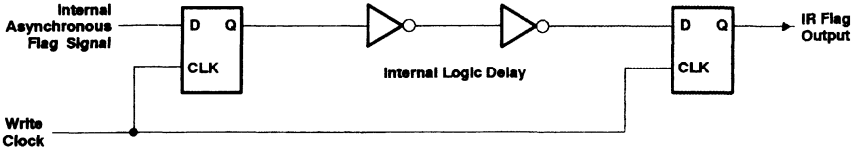



**Figure 3. IR Flag Synchronizer**

The remainder of this discussion will pertain to the metastability performance of the two-stage IR synchronizer, which is the limiting case of the two in terms of MTBF characteristics. As mentioned above, the internal flag signal that goes high on a read and low on a write is synchronized to the write clock through two D-type flip-flop stages. Since this results in the IR flag status of the FIFO being delayed for two clock cycles, a predictive circuit is used to clock the status into the synchronizer at (full minus two) words so that the action of the IR flag going low coincides with the actual full status of the FIFO. However, once the FIFO is full and IR is low, a read that causes the internal flag to go high will not be reflected in the status of the IR flag until two write clocks have occurred.

With the FIFO full and the IR flag low, a read will cause the internal flag signal to go high. This signal will be clocked into the first stage of the two-stage synchronizer on the next write clock. Because these two signals are asynchronous to one another, the potential for the output of the first stage of the synchronizer to go to a metastable state exists. If this condition persists until the next write clock rising edge, a metastable condition could be generated in the second stage and reflected on the IR flag output. This metastable condition manifests itself as a delay in propagation time and is considered a failure only if it exceeds the maximum delay allowed in an application.

The effectiveness of the two-stage synchronizer becomes apparent when attempting to generate failures at a rate high enough to count in a reasonable period of time. As mentioned above, a metastable event generated in the first stage must persist until the next write clock, i.e., when that data is transferred to the second stage. Thus, the resolve time for the first stage is governed by the frequency or period of the write clock. At slower frequencies, the failure rate of the first stage is very low, resulting in a low metastable generation rate to the second stage. The second stage of the synchronizer further reduces the probability of a metastable failure based on the resolve time allowed at the output. The overall failure rate of the device may therefore be affected by increasing the initial asynchronous data generation rate (adding jitter to the data centered about the setup and hold window), by decreasing the resolve time of the first stage (increasing the write clock frequency), and also by reducing the external resolve time at the output.

## Test Setup for Measuring FIFO Flag Metastability

The failure rate of a device can be measured on a test fixture as depicted in Figure 4. The input waveforms used on this setup are also shown in Figure 4. Rising data is jittered asynchronously about the setup and hold aperture of the device under test (DUT) in a +/–400-ps window with respect to the device clock (WCLK). The output of the DUT is then latched into two separate flip-flops, FF1 and FF2, by two different clock signals, CLK1 and CLK2. The resolve time $t_r$ is set by the relationship between CLK1 and WCLK and is measured as the delta between the normal output transition time and the rising edge of CLK1 minus the setup time required for FF1. CLK2 occurs long enough after CLK1 to allow sufficient time for the DUT to have resolved itself to a valid state. The outputs of FF1 and FF2 are compared by the exclusive OR gate, the output state of which is latched into FF3 by CLK3. When a metastable failure occurs, the output of the exclusive OR gate goes high, caused by FF1 and FF2 having opposite data due to the DUT not having resolved itself by time $t_r$. On the next cycle, low data is clocked out of the DUT and into FF1 and FF2 in order to reset the status latch, FF3. Failures are counted for different resolve times, and $\tau$ is then calculated using equation 3.

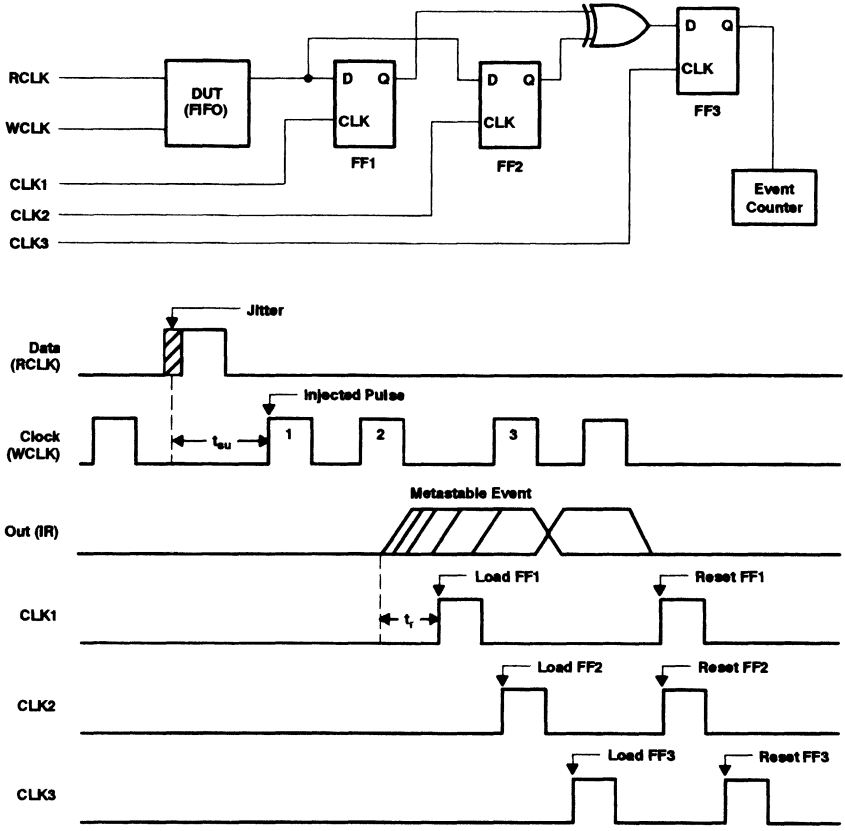



**Figure 4. Metastable Event Counter and Input Waveforms**

Using the test setup described above, failure rates were measured for both an SN74ABT7819 512 × 18 × 2 clocked FIFO and an SN74ACT7807 2K × 9 clocked FIFO. The device is initially written full to set IR low at the boundary condition. A read clock is generated to send the internal flag high, and a jitter signal is superimposed on it to sweep asynchronously with respect to the write clock in an envelope 800 ps wide and centered such that the IR flag goes high alternately on the second and third write clocks following the read clock. The nominal write clock frequency of the test setup is 40 MHz, but to increase the failure rate to an observable level, a pulse is injected into the write clock stream just after the read clock occurs such that the first and second write clocks (the ones that clock the status through the synchronizer) are only 5.24 ns apart. This increases the effective write clock frequency to 191 MHz, reducing the resolve time allowed the first stage and, thus, increasing the failure rate.

This test setup and these actions together create the necessary conditions to generate a metastable occurrence on the IR output that is seen after the second write clock and manifests itself as a delay in propagation time. In this instance, the write clock is the synchronizing clock, and the read clock generates the asynchronous internal data signal. CLK1 was adjusted to vary the external resolve time $t_{r2}$, and the resulting failure rates were recorded.

## Test Results

**SN74ABT7819 Failure Rates†**

| RESOLVE TIME, $t_{r2}$ (ns) | NUMBER OF FAILURES/HOUR | NUMBER OF FAILURES/SECOND | MTBF (SECONDS) |
|---|---|---|---|
| 0.27 | 890 | 0.2472 | 4.04 |
| 0.39 | 609 | 0.1692 | 5.91 |
| 0.53 | 396 | 0.1101 | 9.08 |

† $V_{CC}$ = 4.5 V, $T_A$ = 25°C

After measuring the metastable performance of the ABT7819, some assumptions must be made in order to calculate the parameters $\tau$ and $t_0$. Because the individual flip-flops comprising the two-stage synchronizer cannot be measured separately, it is first assumed that the values for $\tau$ and $t_0$ are the same for both. This is a safe assumption, as these constants are driven by the process technology and because the schematics are identical. The other assumption made involves determining the resolve time allowed in the first stage of the synchronizer ($t_{r1}$). The clock period is set at 5.24 ns, but the delay through the flip-flop and the setup time to the next stage must be subtracted from the clock period to arrive at the true value of $t_{r1}$. These values could not be measured directly and were therefore estimated from SPICE analysis to be 1.3 ns.

Using equation 4 and the measured failure rates to calculate $\tau$ results in a value of 0.33 ns for the conditions given. The following values from the test setup must be used in order to solve for $t_0$:

$t_{r1}$ = 3.94 ns (5.24-ns clock period – 1.3-ns setup and delay time)
$t_{r2}$ = 0.27 ns (set externally at IR output by CLK1)
$f_c$ = 40 MHz
$f_d$ = 125 MHz (4-MHz input adjusted by 25/0.8 jitter ratio)
$MTBF_2$ = 4.04 s

Substituting these values into equation 4 and solving for $t_0$ yields a value of 16.9 ps.

The table below summarizes the results for the SN74ABT7819 and SN74ACT7807 clocked FIFOs. An internal setup and delay time of 1.8 ns was assumed for the SN74ACT7807.

**Values of $\tau$ and $t_0$ for SN74ABT7819 and SN74ACT7807**

| $T_A$ | $V_{CC}$ | SN74ABT7819 | | SN74ACT7807 | |
|---|---|---|---|---|---|
| | | $\tau$ (ns) | $t_0$ (ps) | $\tau$ (ns) | $t_0$ (ps) |
| 25°C | 4.5 V | 0.33 | 16.9 | 0.50 | 1.13 |
| | 5.0 V | 0.30 | 7.0 | 0.40 | 2.05 |
| | 5.5 V | 0.23 | 28.8 | 0.30 | 9.40 |

A word of caution: these numbers indicate the performance of only a few devices and are not intended to represent a fully characterized parameter. However, they should be valid for the purpose of relative performance comparisons, and the values do fall within the expected range given the circuit configuration and process technology in which the devices are fabricated.

## MTBF Comparison

With the constants $\tau$ and $t_0$ now known, calculations of the MTBF of the device under different operating conditions may be performed. First, however, consider an example of the metastability performance of a single-stage synchronizer using equation 2 and the circuit constants $\tau$ and $t_0$ from the measurements above. Assume an application running with a 33-MHz write clock, an 8-MHz read clock, a 9-ns maximum propagation delay time for the IR path, and a 5-ns setup time for IR to the next device. Therefore,

$t_r$ = 16 ns (30-ns clock period – 9-ns propagation delay – 5-ns $t_{su}$)
$f_c$ = 33 MHz
$f_d$ = 8 MHz

Using equation 2 to calculate the MTBF gives $2.55 \times 10^{17}$ seconds, or a little bit more than 8 billion years.

However, the reliability of a one-stage synchronizer degrades as operating frequency increases. With a 50-MHz write clock, a 12-MHz read clock, a 9-ns maximum delay, and a 5-ns setup time,

$t_r$ = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns $t_{su}$)
$f_c$ = 50 MHz
$f_d$ = 12 MHz

Substituting these values into equation 2 yields an MTBF of about 2 hours. This performance is unacceptable, even with a device fabricated in the 0.8-μm BiCMOS process, which is more resistant to metastability than other processes.

The benefits of two-stage synchronization become evident with the next example. Assuming the same conditions stated in the previous case,

$t_{r1}$ = 18.7 ns (20-ns clock period – 1.3-ns setup and delay time)
$t_{r2}$ = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns $t_{su}$)
$f_c$ = 50 MHz
$f_d$ = 12 MHz

Using equation 4 to calculate the MTBF gives $3.16 \times 10^{28}$ seconds, or $1.00 \times 10^{21}$ years.

The table below gives a performance summary of both one- and two-stage synchronizing solutions under different conditions.

**MTBF Comparisons†**

| CONDITIONS | ACT 1-STAGE | ABT 1-STAGE | ACT 2-STAGE | ABT 2-STAGE |
|---|---|---|---|---|
| $f_c$ = 33 MHz, $f_d$ = 8 MHz | 8400 years | $8.1 \times 10^9$ years | $2.62 \times 10^{28}$ years | $4.77 \times 10^{47}$ years |
| $f_c$ = 40 MHz, $f_d$ = 10 MHz | 92 days | 1400 years | $3.56 \times 10^{19}$ years | $2.18 \times 10^{34}$ years |
| $f_c$ = 50 MHz, $f_d$ = 12 MHz | | 2 hours | $4.90 \times 10^{10}$ years | $1.00 \times 10^{21}$ years |
| $f_c$ = 67 MHz, $f_d$ = 16 MHz | | | 417 years | $1.28 \times 10^9$ years |
| $f_c$ = 80 MHz, $f_d$ = 20 MHz | | | | 2900 years |

† Assumptions for the MTBF comparisons:
1) The values for $t_0$ and $\tau$ are those given previously for both the ABT and ACT devices with $V_{CC}$= 4.5 V, $T_A$ = 25°C.
2) Flag propagation delay time (WCLK to IR) is assumed to be 9 ns.
3) Setup times to the next device are 5 ns (up to 50-MHz operation), 4 ns (for 67-MHz operation), and 3 ns (for 80-MHz operation).

## Conclusion

In a digital system, asynchronous operation can cause random errors due to metastability failures under various conditions. Because of their nature, these errors can be very difficult to analyze, but their rate of occurrence (or MTBF of a device) may be predicted to give an indication of overall system reliability. Certain parameters of a device ($t_0$ and $\tau$) are necessary to perform these calculations and are provided herein for both the ABT and ACT families of clocked FIFOs.

Metastability failures in asynchronous systems become increasingly more prevalent at higher operating frequencies. The MTBF comparison clearly indicates the need for addressing these issues with respect to system reliability at operating frequencies in excess of 33 MHz.

With its series of clocked FIFOs, Texas Instruments provides a solution to this problem by synchronizing the boundary status flags with at least two stages to improve the metastable MTBF characteristics over one-stage synchronization. This architecture allows system designers to utilize the high-frequency performance of the device without adversely affecting system reliability due to inadequate synchronization methods.

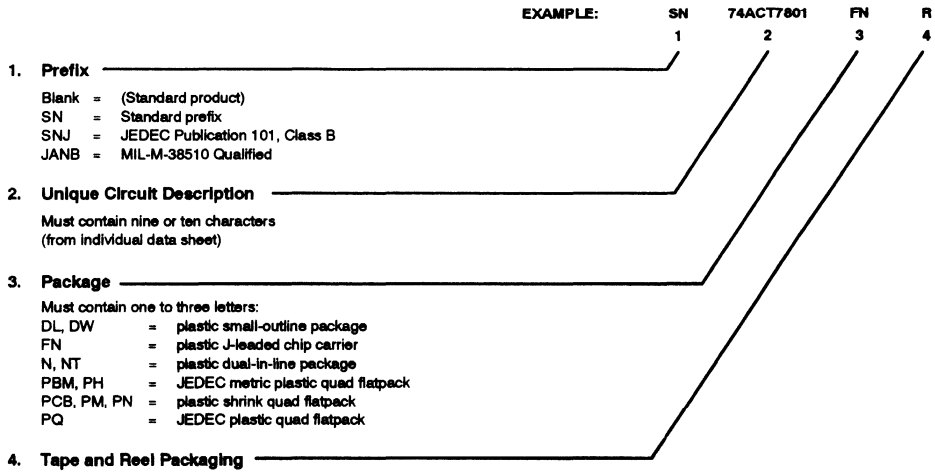
## References


1. J. Horstmann, H. Eichel, and R. Coates, "Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test," IEEE Journal of Solid State Circuits, February 1989, p. 146.
2. H. Veendrick, "The Behavior of Flip-Flops Used as Synchronizers and Prediction of Their Failure Rate," IEEE Journal of Solid State Circuits, April 1980, p. 169.
3. S. T. Flannagan, "Synchronization Reliability in CMOS Technology," IEEE Journal of Solid State Circuits, August 1985, p. 880.
4. T. Kacprzak and A. Albicki, "Analysis of Metastable Operation in RS CMOS Flip-Flops," IEEE Journal of Solid State Circuits, February 1987, p. 59.
5. L. Kleeman and A. Cantoni, "Metastable Behavior in Digital Systems," IEEE Design and Test of Computers, December 1987, p. 4.

## ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

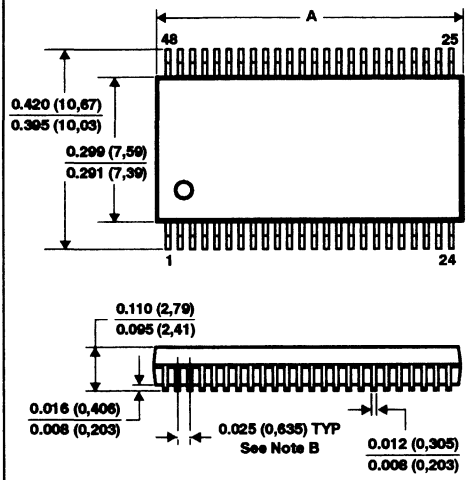


## DL028, DL048, and DL056
## plastic small-outline packages

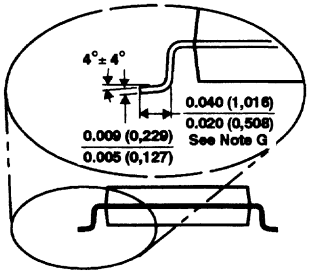
Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

**DL028, DL048, and DL056**
**(48-pin package used for illustration)**

**Designation per JEDEC Std 30:**
**PDSO-G28**
**PDSO-G48**
**PDSO-G56**




| DIM \ PINS | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |



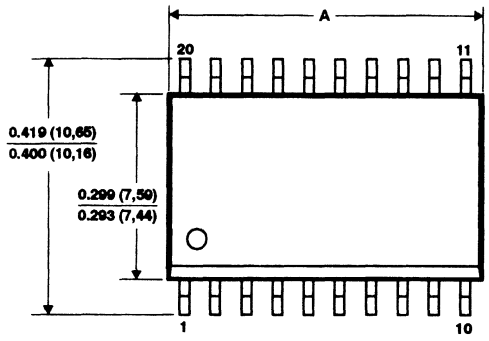

NOTES: A. All linear dimensions are in inches with millimeters in parentheses.
B. Leads are within 0.0035 (0,089) radius of true position at maximum material condition.
C. Lead tips are coplanar within 0.004 (0,102).
D. Body dimensions do not include mold flash, protrusion, or qate burr.
E. Mold flash, protrusion, or qate burr shall not exceed 0.015 (0,381).
F. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
G. Lead length is measured from the lead tip to a point 0.010 (0,254) above the seating plane.

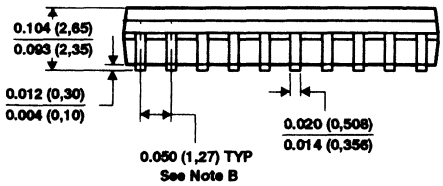
## DW016, DW020, DW024, and DW028
## plastic small-outline packages

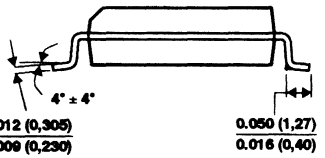
Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require nc additional cleaning or processing when used in soldered assembly.

**DW016, DW020, DW024, and DW028**
**(20-pin package used for illustration)**

**Designation per JEDEC Std 30:**
**R-PDSO-G16**
**R-PDSO-G20**
**R-PDSO-G24**
**R-PDSO-G28**



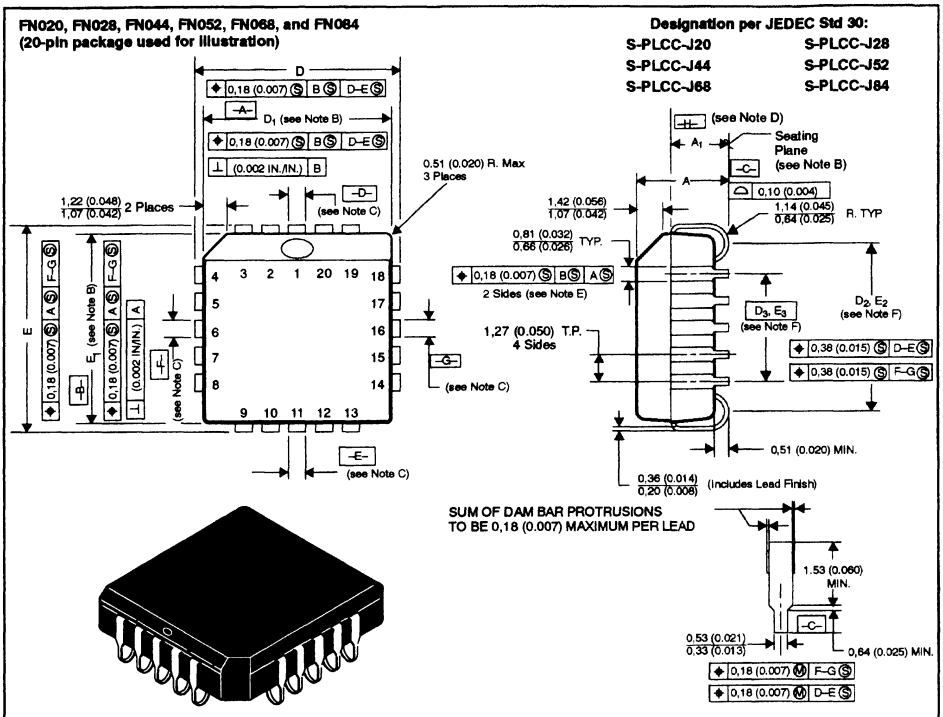




| DIM \ PINS | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (0,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

NOTES: A. All linear dimensions are in inches with millimeters in parentheses.
B. Leads are within 0.005 (0,127) radius of true position at maximum material condition.
C. Lead tips are coplanar within 0.004 (0,102).
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).
F. Interlead flash controlled by TI Statistical Process Control (additional information available through local TI sales office).

## FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carriers

Each of these chip carrier packages consists of a circuit mounted on a lead frame and enncapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.




**(see table on following page for additional dimensions)**

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

B. Dimensions $D_1$ and $E_1$ do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side. Centerline of center pin each side is within 0,10 (0.004) of package centerline by dimension B. The lead contact points are planar within 0,10 (0.004).

C. Datums [D – E] and [F – G] for center leads are determined at datum [– H –].

D. Datum [– H –] is located at top of leads where they exit plastic body.

E. Location of datums [– A –] and [– B –] to be determined at datum [– H –].

F. Determined at seating plane [– C –].

## FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carriers (continued)

| JEDEC OUTLINE | NO. OF PINS | A | | $A_1$ | | D, E | | $D_1$, $E_1$ | | $D_2$, $E_2$ | | $D_3$, $E_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | BASIC |
| MO-047AA | 20 | 4,19 (0.165) | 4,57 (0.180) | 2,29 (0.090) | 3,05 (0.120) | 9,78 (0.385) | 10,03 (0.395) | 8,89 (0.350) | 9,04 (0.356) | 7,37 (0.290) | 8,38 90.330) | 5,08 (0.200) |
| MO-047AB | 28 | 4,19 (0.165) | 4,57 (0.180) | 2,29 (0.090) | 3,05 (0.120) | 12,32 (0.485) | 12,57 (0.495) | 11,43 (0.450) | 11,58 (0.456) | 9,91 (0.390) | 10,92 (0.430) | 7,62 (0.300) |
| MO-047AC | 44 | 4,19 (0.165) | 4,57 (0.180) | 2,29 (0.090) | 3,05 (0.120) | 17,40 (0.685) | 17,65 (0.695) | 16,51 (0.650) | 16,66 (0.656) | 14,99 (0.590) | 16,00 (0.630) | 12,70 (0.500) |
| MO-047AD | 52 | 4,19 (0.165) | 5,08 (0.200) | 2,29 (0.090) | 3,30 (0.130) | 19,94 (0.785) | 20,19 (0.795) | 19,05 (0.750) | 19,20 (0.756) | 17,53 (0.690) | 18,54 (0.730) | 15,24 (0.600) |
| MO-047AE | 68 | 4,19 (0.165) | 5,08 (0.200) | 2,29 (0.090) | 3,30 (0.130) | 25,02 (0.985) | 25,27 (0.995) | 24,13 (0.950) | 24,33 (0.958) | 22,61 (0.890) | 23,62 (0.930) | 20,32 (0.800) |
| MO-047AF | 84 | 4,19 (0.165) | 5,08 (0.200) | 2,29 (0.090) | 3,30 (0.130) | 30,10 (1,185) | 30,35 (1,195) | 29,21 (1,150) | 29,41 (1,141) | 27,69 (1.090) | 28,70 (1.130) | 25,40 (1,000) |

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M–1982.

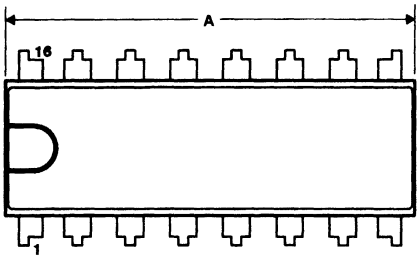
F. Determined at seating plane $\boxed{-C-}$.

## N014, N016, and N020
## 300-mil plastic dual-in-line packages

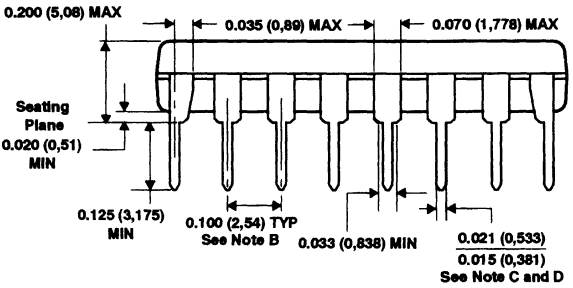
These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note B). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

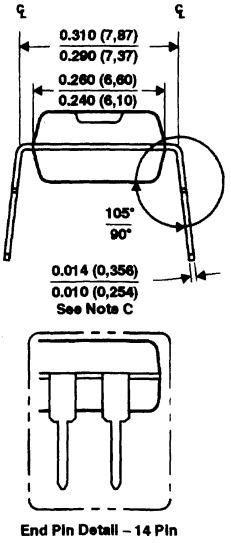
**N014, N016, and N020**
**(16-pin package used for illustration)**

**Designation per JEDEC Std 30:**
**R-PDIP-T14**
**R-PDIP-T16**
**R-PDIP-T20**




| DIM \ PINS | 14 | 16 | 20 |
|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.975 (24,77) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.940 (23,88) |



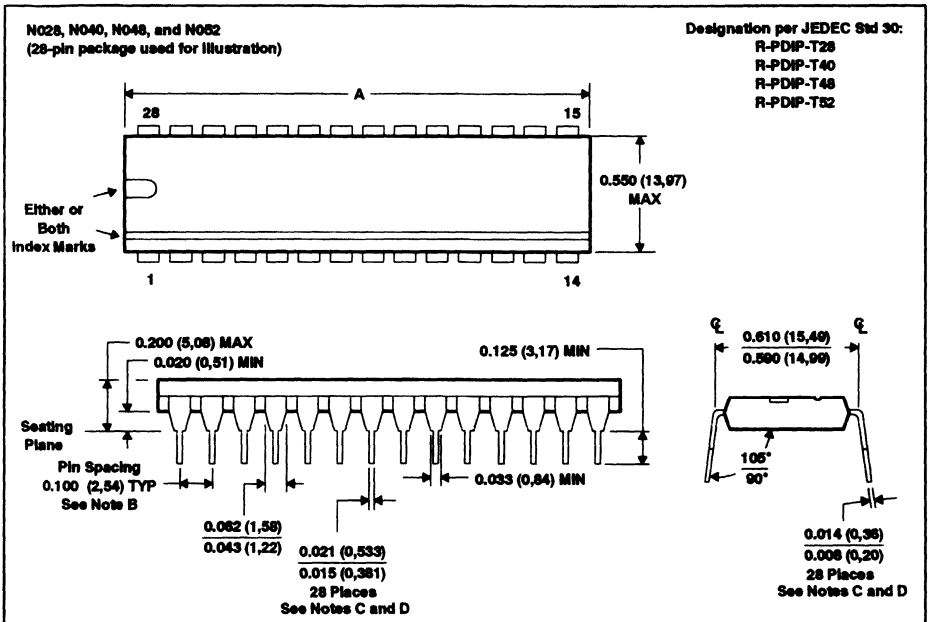



End Pin Detail – 14 Pin

NOTES: A. All linear dimensions are in inches with millimeters in parentheses.
B. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
C. This dimension does not apply for solder-dipped leads.
D. When solder dip is specified, dipped area of the lead extends from the lead tip to at least 0.20 (0,51) above seating plane.

## N028, N040, N048, and N052
## 600-mil plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.600 (15,24) centers (see Note B). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.




| DIM \ PINS | 28 | 40 | 48 | 52 |
|---|---|---|---|---|
| A MAX | 1.440 (36,58) | 2.090 (53,09) | 2.450 (62,23) | 2.650 (67,31) |
| A MIN | 1.380 (35,05) | 2.020 (51,31) | 2.380 (60,45) | 2.580 (65,53) |

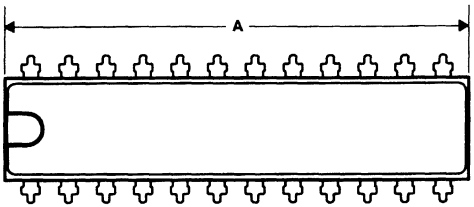
NOTES: A. All linear dimensions are in inches with millimeters in parentheses.
B. Each pin centerline is located within 0.010 (0,25) of its true longitudinal position.
C. This dimension does not apply for solder-dipped leads.
D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,51) above seating plane.

## NT024 and NT028
## 600-mil plastic dual-in-line packages

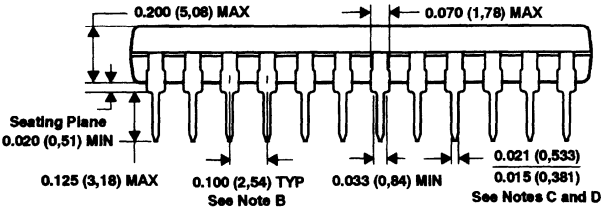
These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note B). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

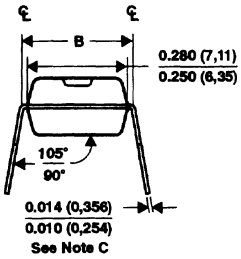
**NT024 and NT028**
**(24-pin package used for illustration)**

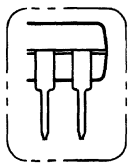
**Designation per JEDEC Std 30:**
**R-PDIP-T24**
**R-PDIP-T28**




| DIM \ PINS | 24 | 28 |
|---|---|---|
| A MAX | 1.260 (32,04) | 1.425 (36,20) |
| A MIN | 1.230 (31,24) | 1.385 (35,18) |
| B MAX | 0.310 (7,87) | 0.315 (8,00) |
| B MIN | 0.290 (7,37) | 0.295 (7,49) |



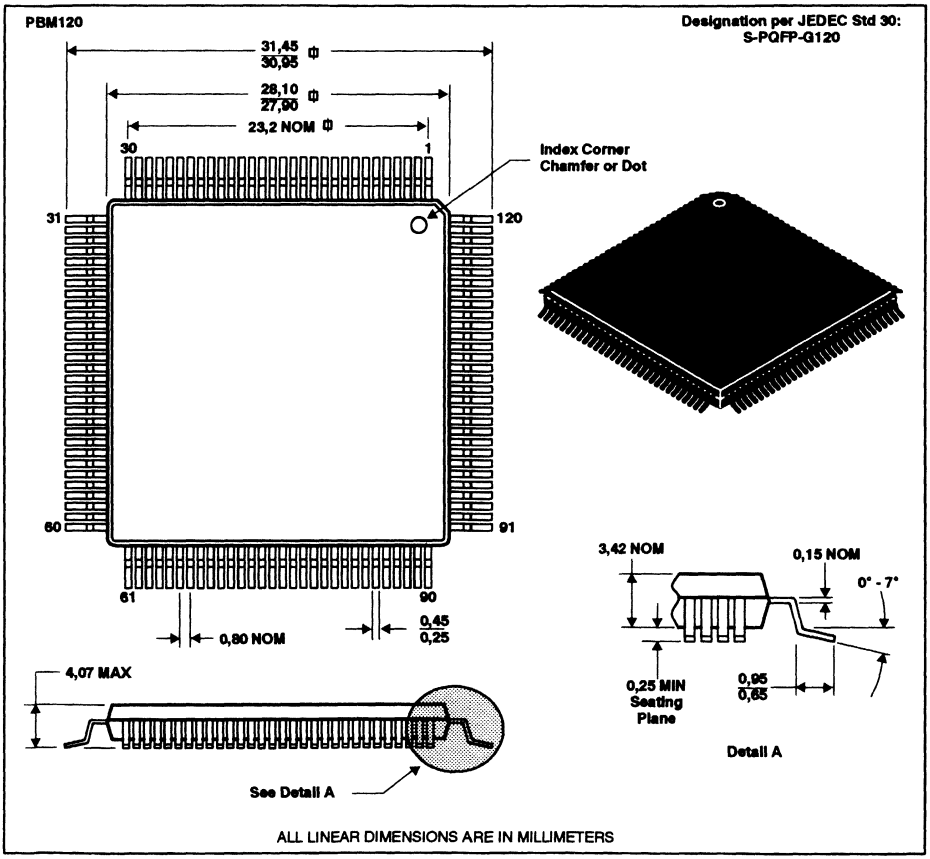



**Alternate Standoff Design**

NOTES: A. All linear dimensions are in inches with millimeters in parentheses.
B. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
C. This dimension does not apply for solder-dipped leads.
D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,51) above seating plane.

## PBM120
## JEDEC metric plastic quad flatpack

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 0,80-mm centers with an 0,80-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.




NOTES: A. Maximum deviation from coplanarity is 0,1 mm.
B. All dimensions and notes for JEDEC outline MO-xxxxxx apply.

## PCB120
## JEDEC metric plastic shrink quad flatpack

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 0,40-mm centers with a 0,535-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.

NOTES: A. All linear dimensions are in millimeters.

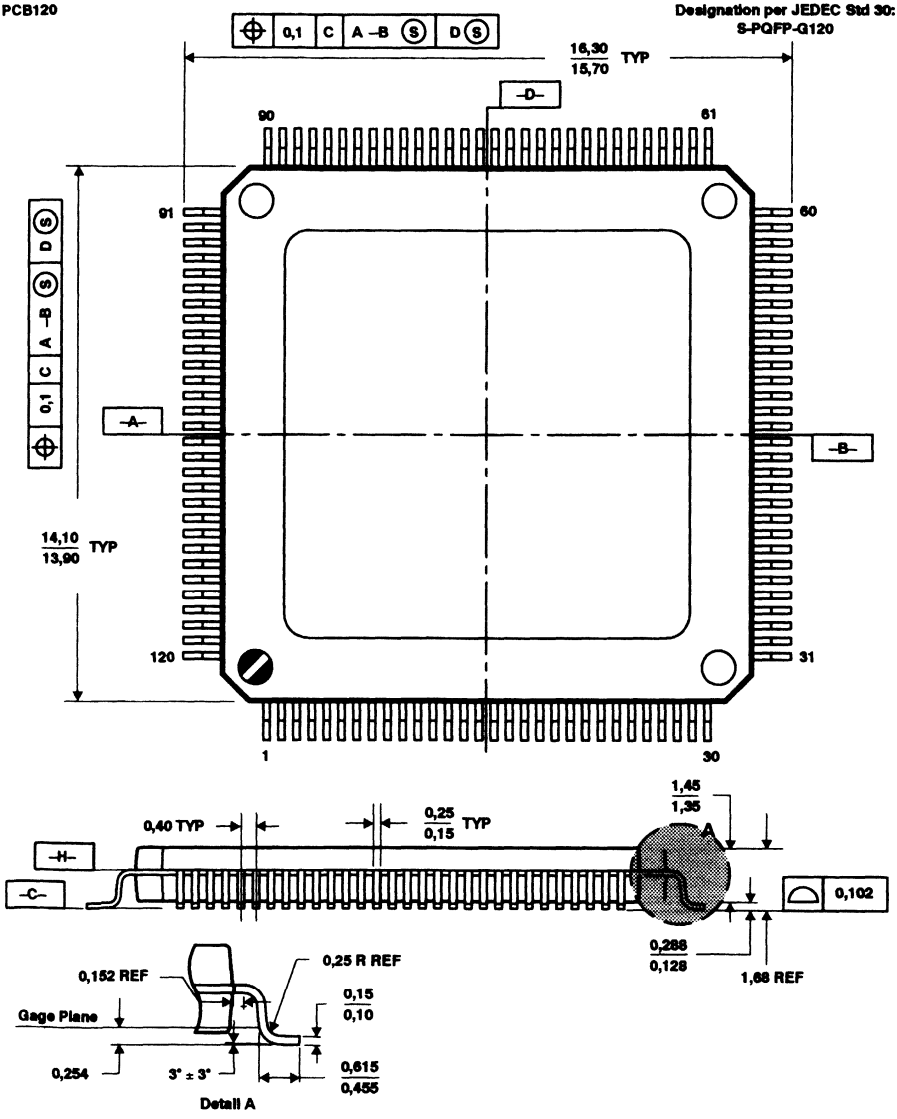
B. Datum plane [-H-] located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.

C. Datum [A-B] and [-D-] to be determined where center leads exit plastic body at datum plane [-H-].

D. Body dimensions (X and Y) do not include mold protrusion. Allowable mold protrusion is 0,253mm.

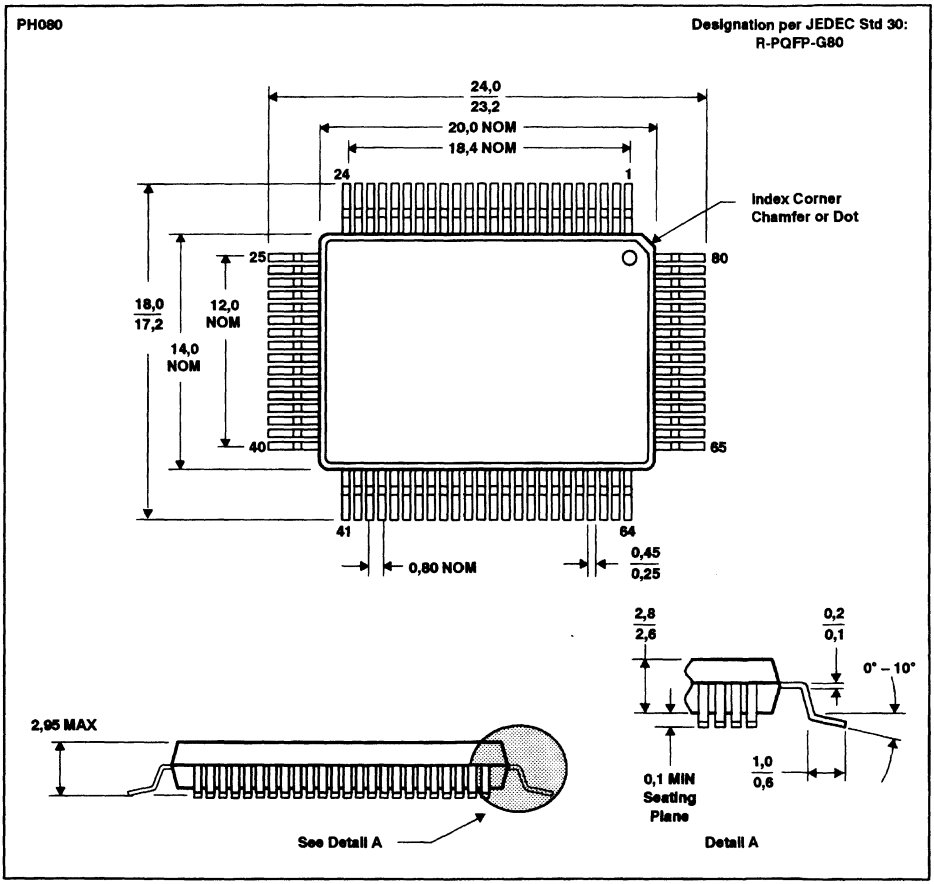
PCB120

Designation per JEDEC Std 30:
S-PQFP-Q120



## PH080
## JEDEC metric plastic quad flatpack

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 0,80-mm centers with a 0,80-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.




NOTES: A. All linear dimensions are in millimeters.
B. Maximum deviation from coplanarity is 0,1 mm.

## PM64, PN80, and PZ100
## JEDEC metric plastic shrink quad flatpacks

These plastic packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 0,50-mm centers with a 0,50-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.

NOTES: A. All linear dimensions are in millimeters.

B. Datum plane [-H-] located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.

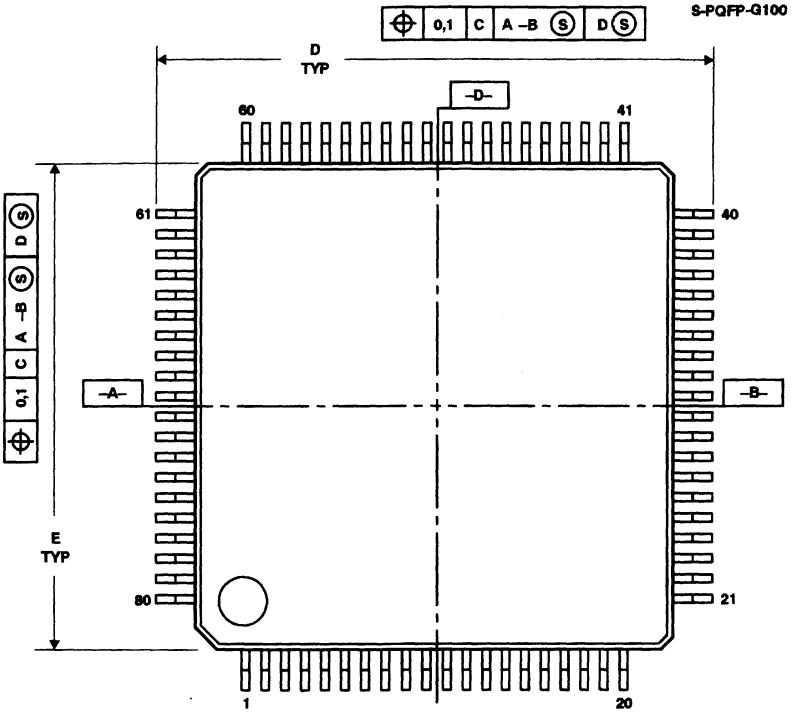
C. Datum [A-B] and [-D-] to be determined where center leads exit plastic body at datum plane [-H-].

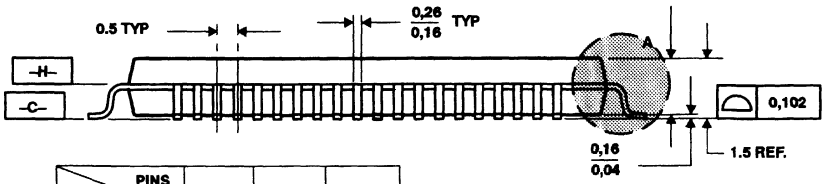
D. Body dimensions (X and Y axis) do not include mold protrusion. Allowable mold protrusion is 0,25mm.

E. When number of leads per side is even, datum are determined by adding half-pitch basic dimension to the centerline of the adjacent lead. When number of leads per side is odd, datum [A-B] and [-D-] are determined by the centerline of the center lead.

**PM64, PN80, and PZ100**
**(80-pin package used for illustration)**

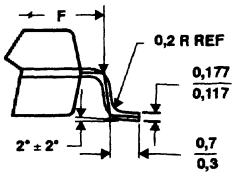
**Designation per JEDEC Std 30:**
**S-PQFP-G64**
**S-PQFP-G80**
**S-PQFP-G100**




| DIM \ PINS | 64 | 80 | 100 |
|---|---|---|---|
| D | 12,2 / 11,8 | 14,2 / 13,8 | 16,2 / 15,8 |
| E | 10,1 / 9,9 | 12,1 / 11,9 | 14,1 / 13,9 |
| F | 10.8 REF | 12.8 REF | 14.8 REF |

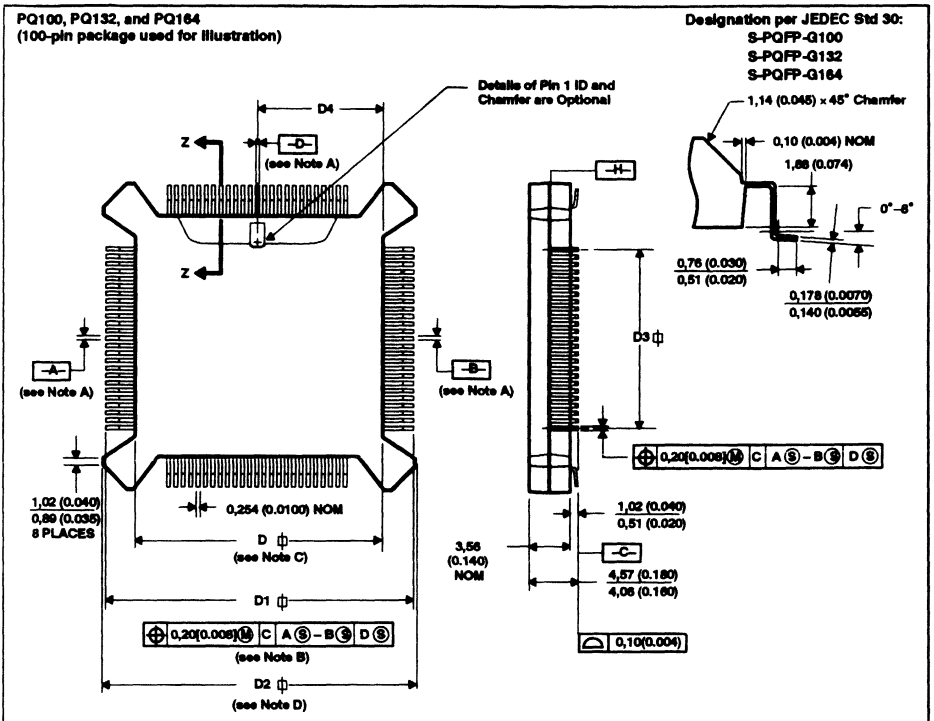
Dimensions apply in both X and Y axis.




Detail A

## PQ100, PQ132, and PQ164
## JEDEC plastic quad flatpacks

These plastic packages consist of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting and leads are spaced on 0,64 (0.025) centers with a 0,64 (0.025) foot length. Leads require no additional cleaning or processing when used in soldered assembly.




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Datums -A-B- and -D- to be determined where center leads exit plastic body at plane -H-.

B. Dimension to be determined at plane -D-.

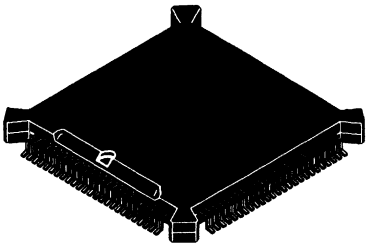
C. Dimension to be determined at plane -H-.

D. Dimension to be determined at plane -H-; dimension does not include 0,254 (0.010) maximum mold protrusion per side.

E. Dimensions and tolerance per ANSI Y14.5M-1982.

F. Tolerances: X,XX±0,12 (X.XXX ±0.005)
X,XXX±0,050 (X.XXXX ±0.002) unless otherwise specified.

**PQ100, PQ132, and PQ164**
**JEDEC plastic quad flatpacks (continued)**



| DIM \ LEADS | | 100 | 132 | 164 |
|---|---|---|---|---|
| JEDEC OUTLINE | | MO-69AD | MO-69AE | MO-69AF |
| D | MAX | 22,48 (0.885) | 27,56 (1.085) | 32,64 (1.285) |
| | MIN | 22,23 (0.875 | 27,31 (1.075) | 32,39 (1.275) |
| D1 | MAX | 19,13 (0.753) | 24,21 (0.953) | 29,29 (1.153) |
| | MIN | 18,97 (0.747) | 24,05 (0.947) | 29,13 (1.147) |
| D2 | MAX | 22,94 (0.903) | 28,01 (1.103) | 33,10 (1.303) |
| | MIN | 22,78 (0.897) | 27,86 (1.097) | 32,94 (1.297) |
| D3 | NOM | 24 @ 0,64 (0.025) = 15,24 (0.600) | 32 @ 0,635 (0.025) = 20,32 (0.800) | 40 @ 0,635 (0.025) = 25,40 (1.000) |
| D4 | MAX | 9,60 (0.378) | 11,99 (0.472) | 14,53 (0.572) |
| | MIN | 9,45 (0.372) | 12,14 (0.478) | 14,58 (0.578) |

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